BIRZEIT UNIVERSITY

**Faculty of Engineering and Technology**
**Department of Electrical and Computer Engineering**

| Course Information | |
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| **Course Title** | **Digital Electronics and Computer Organization Lab** |
| **Course Number** | ENCS 211 |
| **Semester** | First Semester 2016/2017 |
| **Instructors** | Ahmad Afaneh<br>Wasel Ghanem<br>Emad Hamdeh<br>Mohamed Jubran<br>Khader Mohammad<br>Adnan Yahya |
| **Office Hours** | See Ritaj for the office hours of each instructor. Consult with TAs for their office hours. |

## Course Objectives

- To become familiar with basic logic gates and using them to implement digital circuits.
- To study and implement combinational circuits (comparators, adders, decoders…)
- To study and implement sequential circuits (flip-flops, registers, counters…)
- To practice Verilog HDL and Quartus software.
- To become familiar with FPGA programming.
- To implement real FPGA based applications.
- To become familiar with main components and techniques used in computer systems such as ALU, main registers, instruction cycle…
- To became familiar with assembly programming and "Debug" program

**ABET (Accreditation Board for Engineering and Technology) OUTCOMES:**
B: Ability to design and conduct experiments, analyze and interpret data,
C: Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, sustainability political, ethical, health and safety, manufacturability, and
K: Ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

| Assessment Policy | | |
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| **Assessment Type** | **Expected Due Date** | **Weight** |
| **Reports** | Each report is written individually and would include the pre-lab and the post-lab. Some experiment reports may be combined together. 4 reports will be required from each student. | 30% |
| **Quizzes** | Expect one at the beginning of each lab | 15% |
| **Pre-labs /Performance /Discussions** | • You must have your pre-lab solutions with you in order to use them during the experiment. **Do not hand it in. Rather, include it in the report.**<br>• Your performance will be monitored during the lab, and your results may be discussed after the lab.<br>• Post-lab homework will be required in case the report is not required. | 15% |
| **Lab portfolio (keep your lab material: you need to turn it in)** | You are required to hand in a lab portfolio at the end of the semester. It has to include:<br>• lab outline<br>• experiment manuals<br>• corrected reports<br>• pre-labs<br>• corrected quizzes | 5% |
| **Final Exam: Theoretical** | To be announced | 10% |
| **Final practical evaluation** | There will be either a final practical exam or a project. | 25% |

## Experiments:

1 Combinational Logic Circuits ( Introduction-No report)
2 Comparators, Adders and Subtractors
3 Encoders, Decoders, Multiplexers and Demultiplexers
4 Digital Circuit Implementations Using Breadboard
5 Sequential Logic Circuits
6 Counters, Displays and Drivers
7 Introduction to Verilog HDL, FPGA, and Quartus Software
8 System implementations with Verilog
9 FPGA based Security System
10 Simple Computer in Verilog
11 ALU

*The experiment manuals will be posted on Ritaj in due time.*

## Report Format

4 reports are required from each student (see the table above). The report is individual and the report mark will only be given to one student.

Your report must include:

- Objectives
- Brief theoretical review
- Prelab
- All experimental results and circuit schematics.
- Solutions for tasks involved
- Discussion and Evaluation
- Conclusions

## ميثاق شرف الأمانة الأكاديمية

**بموجب التسجيل في هذا المساق يلتزم الطالب باحترام أنظمة وقوانين الجامعة وخاصة تلك المتعلقة بالأمانة العلمية وعدم الغش. ويتحمل الطالب مسئولية ذاتية، أدبية وقانونية، عن المحافظة على الأمانة العلمية وذلك بالامتناع عن الغش في الامتحانات والوظائف والتقارير، وعدم السماح لغيره من الطلاب بأن ينقلوا عنه في الامتحانات والوظائف والتقارير.**

**يستوجب الغش أو محاولة الغش التوبيخ والإجراءات القانونية المنصوص عليها في تعليمات الأمانة الأكاديمية التي أقرها مجلس الجامعة، وتشمل ما يلي:**

1. **العقوبة الأكاديمية: يقررها مدرس المساق وقد تصل إلى علامة رسوب في المساق.**
2. **العقوبة التأديبية: تقررها لجنة النظام في الكلية وقد تصل إلى الفصل المؤقت أو النهائي من الجامعة.**

**بموجب تسجيلي في هذا المساق واستلامي لهذا الميثاق أتعهد أمام الله أن أحافظ على الأمانة الأكاديمية بأن أمتنع عن الغش، وأن لا أتسامح مع أي محاولة للغش من قِبل الآخرين.**