ENCS-211

A Guide to Writing the 5th Experiment

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This is a guide for writing the 5th experiment. Follow the following rules and do NOT include any extra information (solutions to discussion or tasks) than the ones requested.

Use Times New Roman, 12pt size and line spacing of 1.5.

Restriction: Theory must NOT exceed a single page (you will lose points if it did).

I. Theory

Definition of sequential logic circuits.

I.1 Latches and Flip-Flops

Definition of a latch. [1]
Definition of a flip-flop. [2]

I.2 Registers

Definition of a serial shift register. [3]
Definition of parallel load register. [4]

I.3 Counters

Definition of a ripple counter. [5]
Definition of a synchronous counter. [6]

II. Experiment Outline

II.1 Latches and Flip-Flops

A) Constructing RS latch with Basic Logic Gates
B) Constructing RS latch with control input
C) Constructing D latch with RS latch
D) Constructing JK latch with RS latch
E) Constructing JK Flip-flop with master- slave RS latches

II.2 Registers

A) Constructing Shift Register with D Flip-Flops
B) 4-Bit Shift Register with serial and parallel load
1. Shift- right serial- input
2. Parallel- load Register

II.3 Counters

A) 2-bit Synchronous Counter
B) 3-bit (divide-by-eight) Ripple Counter
C) BCD Counter
D) Divide-by-8 counter using BCD chip counter

III. Procedure, Results and Discussions

NOTE: Provide extra column for all latches/flip-flops part to indicate the state (set, reset... etc.)
Warning: Do not copy instructions from manual. Do not provide re-phrased instructions, Do not provide useless details. Example (do not do this): "We used KL-26006 module to construct the circuit shown in Figure.14. We connected CK2 to **Pulser switch**. Then followed the sequences in Table 5.5"

Section/Part	Required
III.1 Latches and Flip-Flops	
A) Constructing RS latch with Basic Logic Gates	Explain drawback of this latch type.
B) Constructing RS latch with control input	Explain enhancement of adding control input.
C) Constructing D latch with RS latch	Simple comment on how it works.
D) Constructing JK latch with RS latch	Simple comment on how it works.
E) Constructing JK Flip-flop with master- slave RS latches	Simple comment on how it works.
III.2 Registers	
A) Constructing Shift Register with D Flip-Flops	Explain inputs: A, B and CK. How you managed to utilize them to make a shifting process.
B) 4-Bit Shift Register with serial and parallel load	Explain inputs: Serial, Mode, CK, and Load.
1. Shift- right serial- input	Explain how you managed to achieve a serial shift.
2. Parallel- load Register	Explain how you managed to achieve parallel load.
III.3 Counters	
A) 2-bit Synchronous Counter	Provide how it works.
B) 3-bit (divide-by-eight) Ripple Counter	Provide how it works.
C) BCD Counter	Explain the two reset inputs.
D) Divide-by-8 counter using BCD chip counter:	Explain how you managed to make it count just to 8.

IV. Conclusions

Warning: Do not provide summaries.

Conclusions ideas may cover:

When to use a latch, when to use a flip-flop?

What enhancement does a JK flip-flop have over RS?

What is the trade-off between serial shift and parallel load registers? When to use each?

When to use a ripple counter? A synchronous counters?

How to make any counter count from 0 to N? What thing is needed to be done?

References

[1]
[2]
[3]
[4]
[5]