

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

**ENCS 211**

**Digital Electronics and Computer Organization Lab**

**Experiment #2**

**Comparators, Adders and Subtractors**

**Student’s names: Ahmad Salah**

**Student’s id’s: 1130083**

**(1)Abstract:**

In this experiment we will show you how to construct a half and full adders, half and full subtractors and a comparators.

We implement them using a basic logic gates and IC,

**(2)Theory:**

**(4.1)**

comparator: a comparator has 3 outputs (a<b,a=b,a>b), we use 4-bit comparator to compare to binary numbers with each other, it works by starting compare the most significant bits with each other, depends on the value of each number (a,b) if it’s not the same it gives value (1) to (a>b) or (a<b) but if it’s the same it moves on to the next bit and compare them as it did with the first bit and so on, till it reaches the last bit, if (a) and (b) have the same value it gives value (1) to (a=b).

**(4.2)**

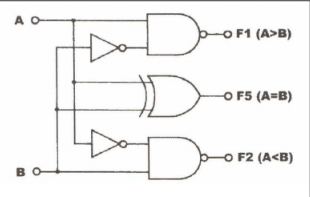
* half-adder: the half-adder is used to add two bits, therefor it has 2 input (a,b) and 2 outputs (s,c), where s = a (XOR) b and c = a (AND) b which make it a carrier, as you can see, there is two logic gates are used in the half-adder (and, xor) gates.
* full-adder: basically the full-adder is mad of two half-adders, it has three inputs (a,b, Cin) and two output (S,Cout), we use full-adder because its useful to add three bits, but the half-adder can’t does that, the sum (S) is taken from XOR gates and the carrier ( c ) by OR gates.

**(4.3)**

* half-subtractor: the half-subtractor has two inputs (a,b) and two outputs  (DF,BW) to get the DF we use XOR gates and the BW by using AND gates.
* full-subtractor: the full-subtractor is a combination of XOR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor .The first half-subtractor will be C and A B. The output will be difference output of full-subtractor.

***3)Procedure :***

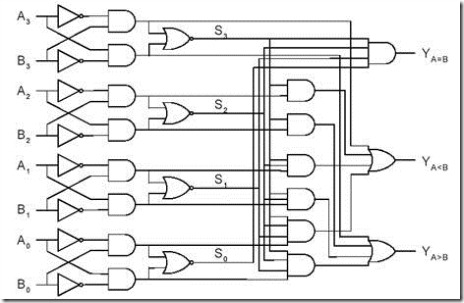
**(5.1)**Comparator :



**1-bit Comparator Design**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Inputs | |  | Outputs | | |
| B | A | F1 | F2 | F5 |
| 0 | 0 | A=B | 1 | 0 | 0 |
| 0 | 1 | A>B | 0 | 1 | 1 |
| 1 | 0 | A<B | 1 | 1 | 1 |
| 1 | 1 | A=B | 1 | 0 | 0 |

**1-bit Comparator truth-table**

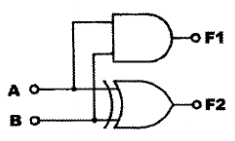
****

**4-bit Comparator Design**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | | | | | |  | **Outputs** | | |
| **A4** | **A3** | **A2** | **A1** |  | **B4** | **B3** | **B2** | **B1** | **A>B** | **A<B** | **A=B** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **0** | **0** |

**4-bit Comparator Truth-table**

**(5.2.1) half-adder:**

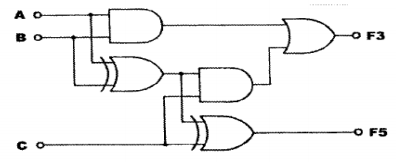
****

**Half-Adder Design**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs | |  | outputs | |
| Sw1(B) | Sw0(A) | F1(carry) | F2(sum) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |

**Half-Adder Truth Table**

**(5.2.2) Full-Adder**

****

**Full-Adder Design**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | |  | **Outputs** | |
| Sw3(C) | Sw2(B) | Sw1(A) | F3(carry) | F5(sum) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Full-Adder Truth Table**

***(5.2.3) 4-bit Full-Adder:***

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | |  | **Outputs** | |
| Y | X | ∑ | F1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 6 | 6 | 0 |
| 0 | 9 | 9 | 0 |
| 0 | F | F | 0 |
| 1 | 3 | 4 | 0 |
| 1 | 6 | 7 | 0 |
| 1 | 8 | 9 | 0 |
| 3 | 6 | 9 | 0 |
| 4 | 8 | C | 0 |
| 4 | F | 3 | 1 |
| 8 | 7 | F | 0 |
| 9 | 9 | 2 | 1 |
| A | B | 5 | 1 |
| C | E | A | 1 |
| F | F | 0 | 1 |

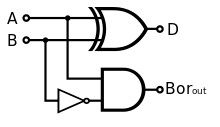
**4-bit Full-Adder Truth Table**

***(5.2.4) BCD-Adder:***

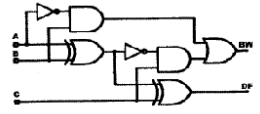
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | | | | |  | **Outputs(U5)** | | | | | **Final(U9)** | | | | | |
| **X3** | **X2** | **X1** | **X0** | **Y3** | **Y2** | **Y1** | **Y0** | **F1** | **F11** | **F10** | **F9** | **F8** | F2 | **F3** | **F7** | **F6** | **F5** | **F4** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** |
| **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** |
| **0** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **0** | **0** |

**BCD-Adder Truth Table**

***(5.3.1) Half/full-subtractor:***

****

**Half-subtractor Design**

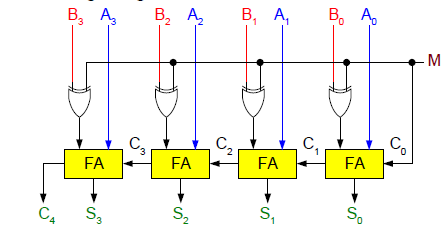
****

**Full-subtractor Design**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | |  | Outputs | | | |
| C | A | B | F1(BW1) | F2(DEF1) | F3(BW2) | F4(DEF2) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |

**Half/Full-subtractor Truth Table**

***(5.3.2) 4-Bit Full-Subtractor:***

****

**4-bit Full-Subtractor Design**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | | | | | | | Borrow | Difference | | | |
| X3 | X2 | X1 | X0 |  | Y3 | Y2 | Y1 | Y0 | F1 | F11 | F10 | F9 | F8 |
| 0 | 1 | 0 | 0 |  | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 |  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |  | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

**4-bit Full-Subtractor Truth Table**

***Conclusion:***

After implementing comparable, half/full adders, and half/full subtractor, it is shown that these constructors are very useful, especially in calculators, and computer programs.

During implementing we faces some problems, for example as we were implementing BCD-Adder we accidently connected the X’s in the place of the Y’s and opposite for the Y’s, after we completed filling the truth table for the BCD-adder we noticed that, but the interesting part that when we replaced Y’s by the X’s, and the X’s by the Y’s we got the same result in the outputs.