

**Experiment.No.8**

**Verilog: Part II**

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**1) Abstract:**

**In this experiment we connected the counter and the 7 segments and frequency division together so we can get counter with a good speed that we can see the changing in the numbers, and then we should construct multipliers signed and unsigned ones.**

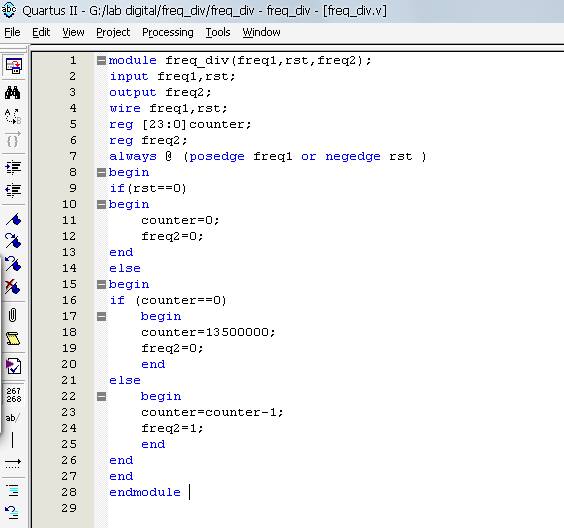
**2) Table of contents:**

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**3) Procedure:**

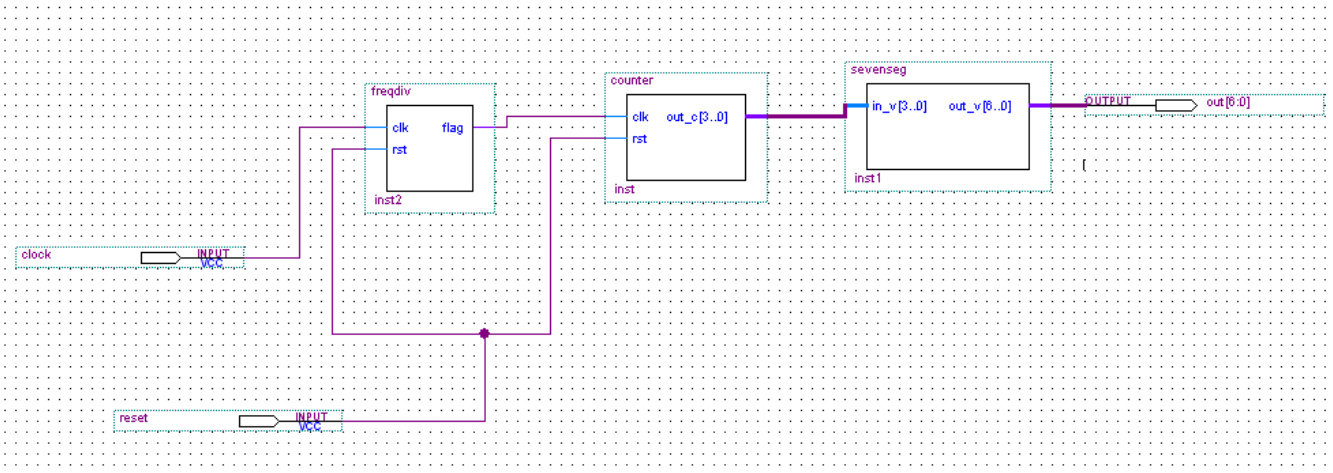
**3.1) Frequency division:**

**The speed of the counter can be manipulated my changing the frequency rate, so the counter speed can be slowed down by increasing the ratio. In this case we want to run it at 27 Mhz, so by the ratio the counter should be set to 13.5 mil and the range for this number is 24 bit, as it shown in the code below.**

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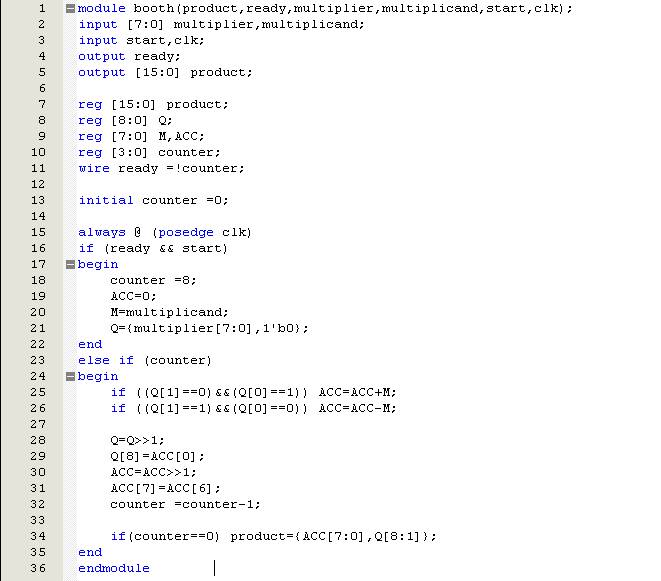
**3.2) Counter system:**

**After building the frequency division we made symbol of it and get the symbols of the counter that we did previously and the 7 segments from the previous lab, then all the symbols should be connected to each other, and there should be 2 inputs (clock and reset), and there is 7 output from the 7 segments witch gives one number in decimal, and the connection is done as it shown below.**

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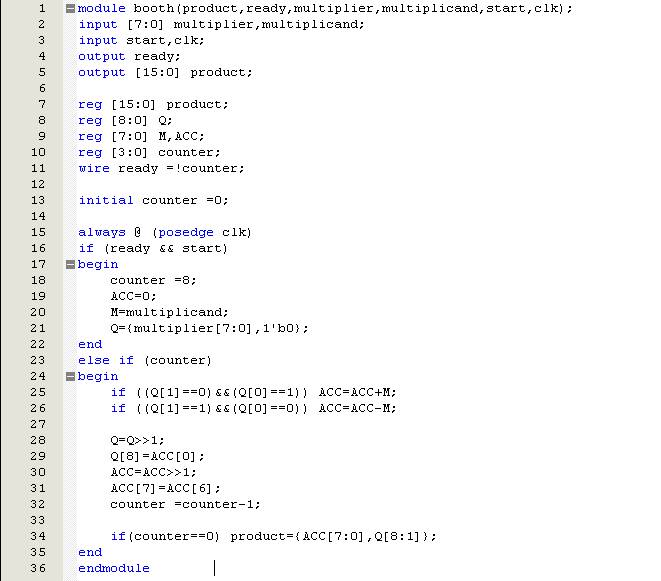
**3.3) Unsigned multiplier:**

**The unsigned multiplier by using this code:**

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**3.4) Booth:**

**Booth is used to multiply two sign binary numbers, and it can be constructed as it shown in the code below.**

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**4) Conclusion:**

**In this experiment we learned how to adjust the frequency so we can make the counter work at the speed and in the way the we want, and by implementing the unsigned multiplication and the booth, we understand the difference much better, and we now have some ideas when we should use each kind of the multiplication in the future.**