

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

**ENCS 211**

**Digital Electronics and Computer Organization Lab**

**Prelab-Experiment #3**

**Encoders, Decoders, Multiplexers and Demultiplexers**

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***(2-a)***

*Y= f(A, B, C) = AB’+B’C*

*f(A,B,C) = AB'(C+C') + (A+A')B'C*

*f(A,B,C)* = AB'C + AB'C'+ AB'C+ A'B'C

*f(A,B,C)* = Σ(1,4,5)

|  |  |  |  |
| --- | --- | --- | --- |
| A | *B* | *C* | *Y* |
| *0* | *0* | *0* | *0* |
| *0* | *0* | *1* | *1* |
| *0* | *1* | *0* | *0* |
| *0* | *1* | *1* | *0* |
| *1* | *0* | *0* | *1* |
| *1* | *0* | *1* | *1* |
| *1* | *1* | *0* | *0* |
| *1* | *1* | *1* | *0* |

**(2-b)**

The input connections necessary to implement the function in part (a) is shown in figure (1).

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Figure (1): 8-to-1 MUX.

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**(3-a)**Convert the following expression into summation form:

Y = A'BC +BC'

Y = A'BC +BC' = A'BC + (A+A') BC'

Y = A'BC + ABC' + A'BC'

Y = Σ (2, 3, 6)

**(3-b)**  The demultiplexer output is selected, and will go low, by the address of inputs A, B, C when the IC is enabled .therefore, we can create the output function Y by summing together the outputs indicated by the summation form above. Since the outputs of the demultiplexers are active–low, this is done with a NAND gate. Connect each of the true minterms output of the demultiplexer to an input of the NAND gate, connect all unused NAND inputs to logic 1.

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Figure (2): 3-to-8 DeMUX.