

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

**ENCS 211**

**Digital Electronics and Computer Organization Lab**

**Experiment 2**

**Comparators, Adders and Subtractors**

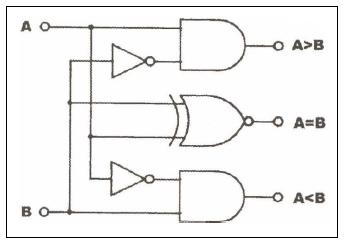
1. **Objectives** 
   1. To understand the construction and operating principle of digital comparators.
   2. To construct comparators with basic gates and IC.
   3. To implement half- and full adders using basic logic gates and IC.
   4. To understand the theory of complements.
   5. To construct half- and full- subtractor circuits.
2. **Apparatus** 
   1. KL-22001 Basic Circuit Lab.
   2. KL-26001 Combinational Logic Circuit Experiment Module (1).
   3. KL-26002 Combinational Logic Circuit Experiment Module (2).
   4. KL-26005 Combinational Logic Circuit Experiment Module (5).
3. **Pre Lab**

Prepare all sections and work out all the required designs.

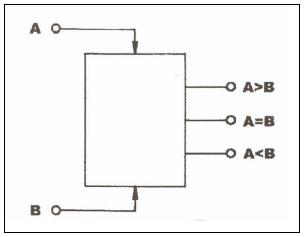
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| --- | --- | --- |
| **1.4** | **Theory** |  |
| **1.4.1. Comparator Circuit** | |  |
| At | least two numbers are required | to perform any comparison. The |
| simplest form of the comparator has | | two inputs. If the two inputs are |

called A and B, there are three possible outputs: A>B, A=B, an d A<B. **Fig1.1** shows the schematic andsymbol of a simple comparator.

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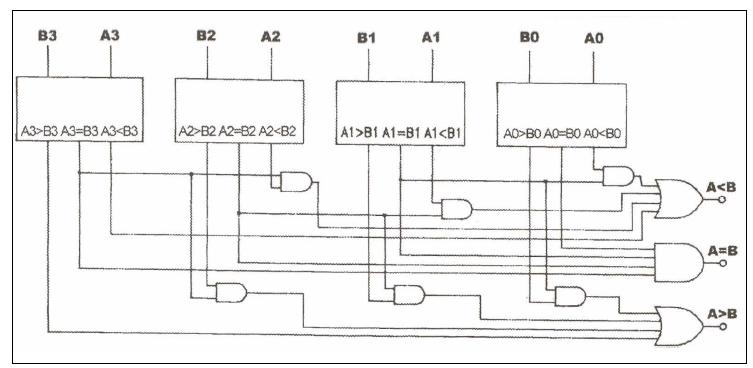
(a) Logic Diagram



(b) Circuit symbol

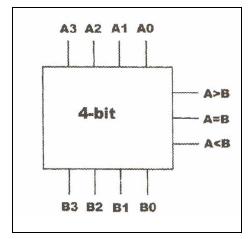
**FIG 1.1: Comparator**

In actual applications 4-bit comparators are used most often. In a 4-bit comparator, each bit represents 20, 21, 22, *and* 23. Comparison will start from the most significant bit ( 23 ), if input A is greater than input B at the 23 bit, the “A>B” output will be in high state. **Fig 1.2** shows the schematic and symbol of 4 bit comparator.



(a) Constructed with four 1-bit Comparators

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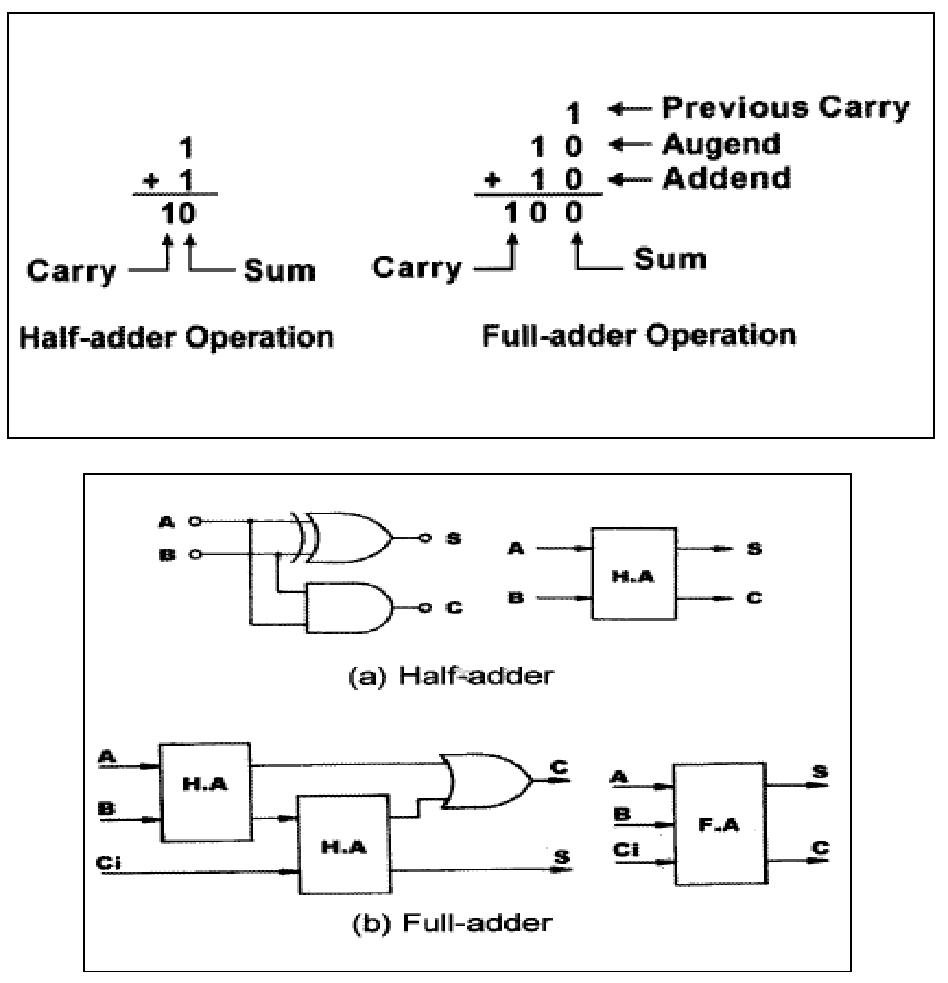


(c) Circuit Symbol

**FIG1.2: 4-bit Comparator**

**1.4.2. Half- and Full- Adder Circuits**

Digital computers perform a variety of information processing tasks. Among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition of two binary digits. Combinational circuit that performs the addition of two bits is called a half adder. One that performs the addition of three bits (two significant bits and previous carry) is a full adder. The names if the circuits stem from the fact that two half adders can be employed to implement a full adder.



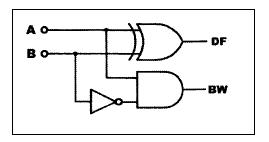
**FIG 1.2: Half – and full- adders**

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**1.4.3. Half- and Full-Subtractor Circuits**

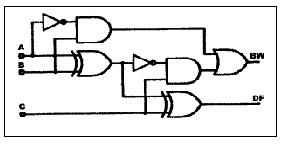
Binary subtraction is usually performed by using 2’s complement. Two steps are required to obtain 2’s complement. First, the subtrahend is inverted to 1’s complement, i.e. a “1” to a “0” and a “0” to a “1”. Secondly, a “1” is added to the least significant bit of the subtrahend in 1’s complement.

A half-subtractor performs the task if subtraction 1-bit at a time regardless of whether the minuend is greater or less than the subtrahend. “Borrow” from previous subtraction is not taken into consideration.



**FIG 1.3: Half-Subtractor**

The full-subtractor has to consider borrow(s) from previous stages.



**FIG 1.4: Full-Subtractor**

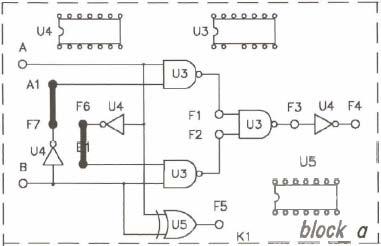
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1. **Procedure**

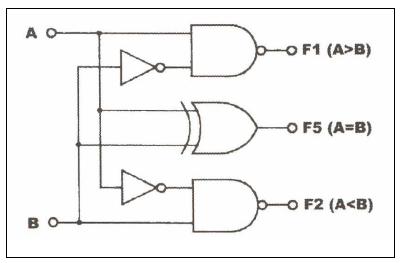
**1.5.1. Comparator Circuits**

**A. Constructing Comparator with Basic Logic Gates**

1. Set the KL-26001 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block a**. Complete the connections by referring to wiring diagram in **Fig 1.5(a)** and the logic diagram in **Fig1.5 (b).**



(a) Wiring diagram (KL-26001 block a)

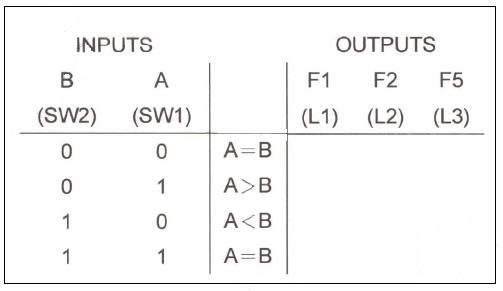


(b) Logic Diagram

**FIG 1.5: 1-bit comparator**

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1. The inputs are active high. Connect inputs A and B to Data Switches SW1 and SW2. The outputs are active low. Connect outputs F1, F2, F5 to logic Indicators L1, L2, L3, respectively. Apply +5 VDC from the Fixed Power on KL-26001 Module.
2. Follow the input sequences in **Table 1.1**. Observe and record the outputs.

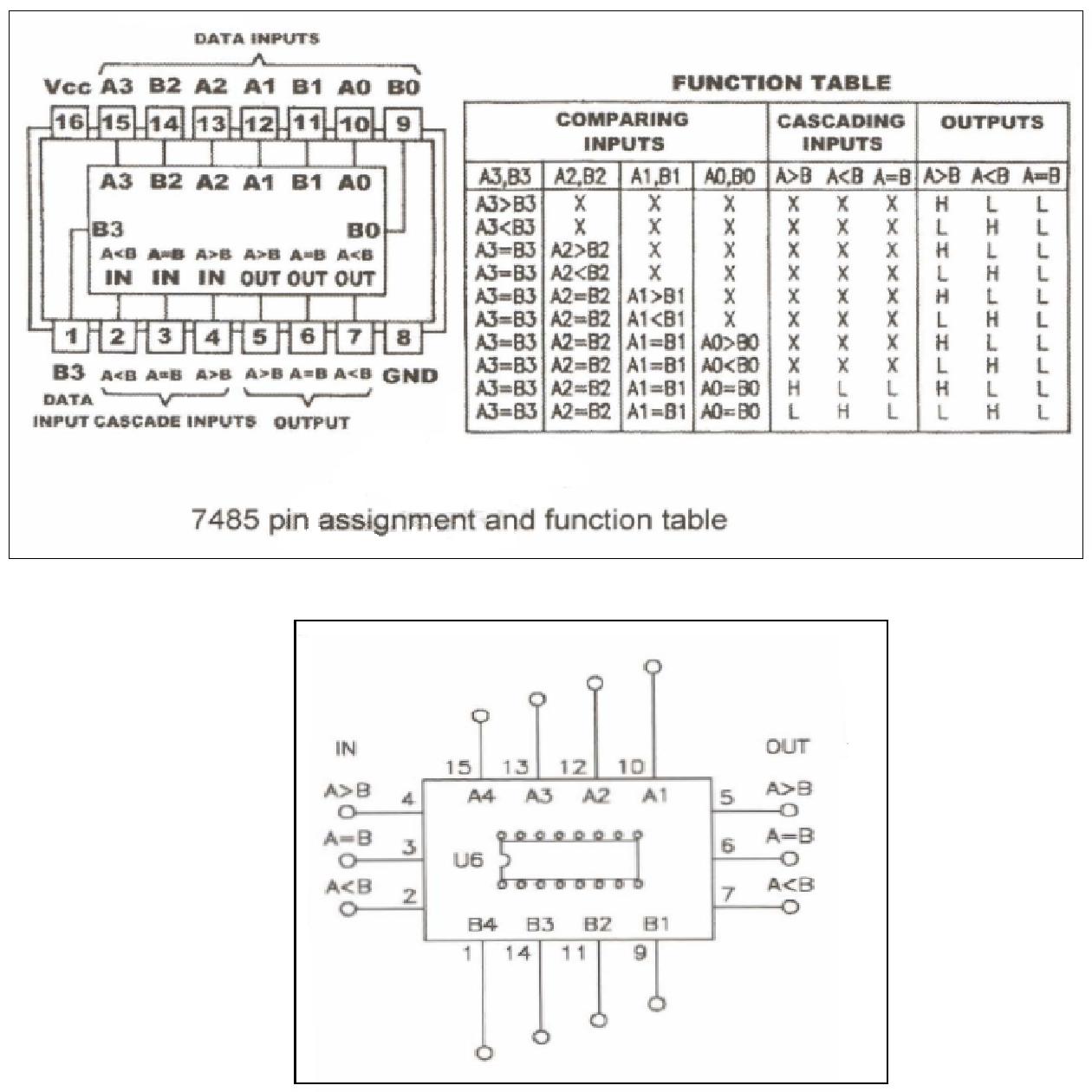


**Table 1.1**

**(B) Constructing Comparator with TTL IC**

1. Set the KL26005 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block a.** Apply +5VDC from the Fixed Power on KL-22001 Lab to KL26005 Module. **U6** is a 7485 4-bit comparator IC. Its pin assignment and function table are given below.

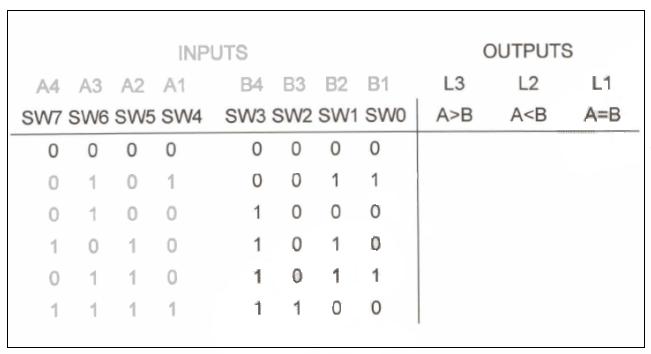
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**FIG1.6: 26005 block a**

1. Connect the inputs A1~A4 to SW4 ~ SW7 and B1 ~ B4 to SW0 ~ SW3, respectively.
2. Connect the outputs A=B to L1, A<B to L2, and A>B to L3.
3. Follow the input sequences in **Table1.2**. Observe and record the outputs.

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**Table 1.2**

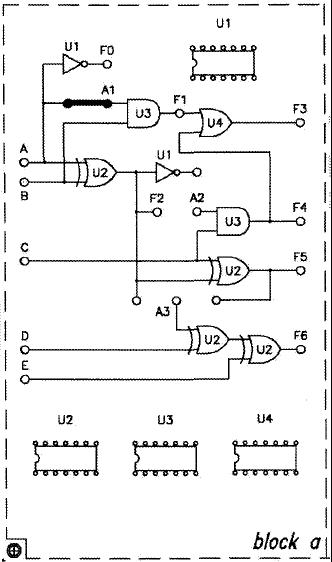
Design a three-bit comparator (using the basic comparator) and hand it out to your TA. **(Pre Lab)**

1. **Half- and Full-Adder Circuits** 
   1. **Constructing Half- and Full-Adders with Basic logic Gates**

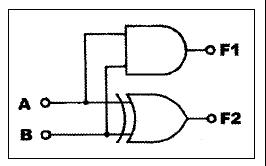
Hand out, Design, Boolean function, and truth table of half- and full-adder to your TA. **(Pre Lab)**

1. Set the KL-26002 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block a**.
2. Complete the connections by referring to the wiring diagram in **Fig1.7 Apply** +5VDC from Fixed Power on the KL-22001 Lab to KL-26002 Module.

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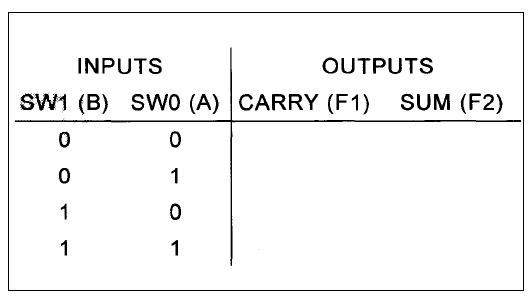
**FIG1.7: Wiring Diagram (KL-26002 Block a)**



**FIG1.8: Half-Adder Circuit**

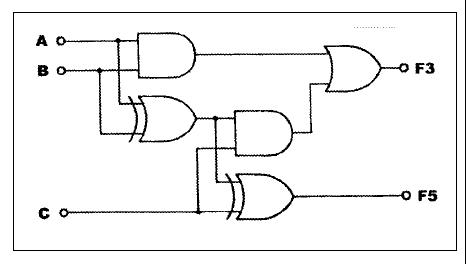
1. Connect inputs A and B to Data Switches SW0 and SW1, respectively. Connect output F1 and F2 to logic Indicators L1 and L2.
2. Follow the input sequence for A and B in **Table1.3** and record the output states.

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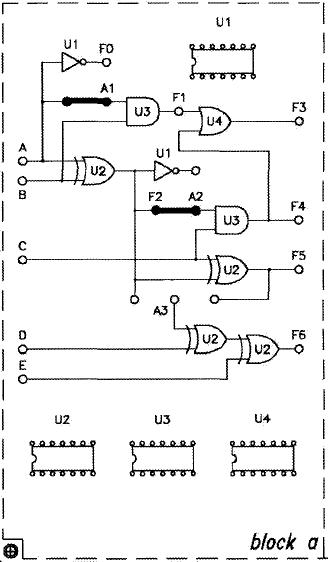
**Table1.4**

1. Complete the connections by referring to the wiring diagram in **Fig1.10** and the full-adder circuit in **Fig1.9.**



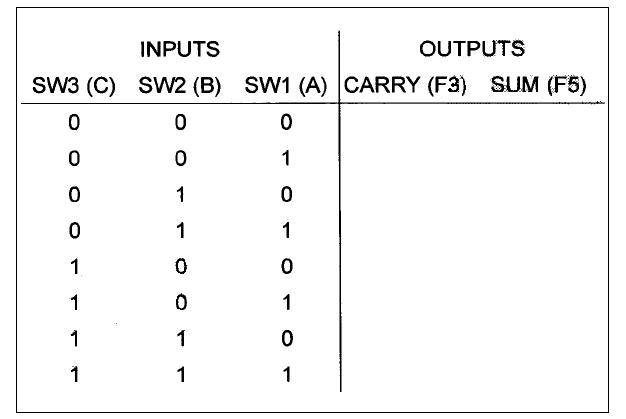
**FIG1.9: Full-Adder Circuit**

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**FIG1.10: Wiring Diagram (KL-26002 Block a)**

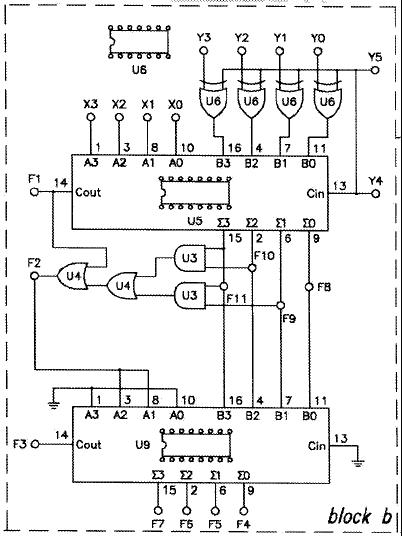
1. Connect A, B, and C to SW1, SW2, and SW3. The input A represents the augend, input B the addend, and the C is the previous carry. Connect outputs F3 and F5 to Logic Indicators L1 and L2, respectively.
2. Follow the input sequence in **Table1.5** and record the output states.



**Table1.5**

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1. **Constructing 4-Bit Full-Adder with IC** 
   1. Set the KL-26002 Module on the KL-22001 Basic Electricity Lab, and locate **block b.** The **U5,** 7483 is a 4-bit binary adder. Connect input Y5 to ground “0”, so the XOR gates of **U6,** which are connected to Y0~Y3, will act as buffers.
   2. Connect inputs X0~X3 (addend) and Y0~Y3 (augend) to Data Switches SW0~SW3 and SW4~SW7 respectively. Connect F1 (Carry out) to L1 and ∑0 ~ ∑3 (sum) to L2~L5. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26002 Module.



**FIG1.11: Wiring Diagram (KL-26002 block b)**

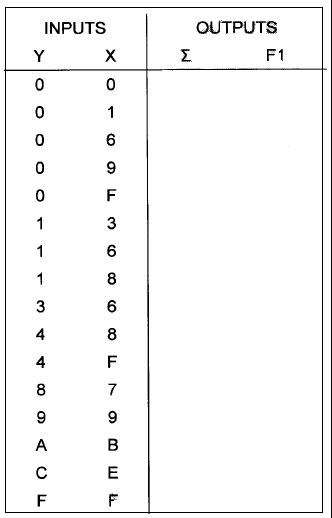
12

1. Follow input sequences in **Table 1.6** and record the outputs F1 in binary and ∑ in hexadecimal.

**X=X3X2X1X0**

**Y=Y3Y2Y1Y0**

* + = ∑3∑2∑ 1∑0



**Table 1.6**

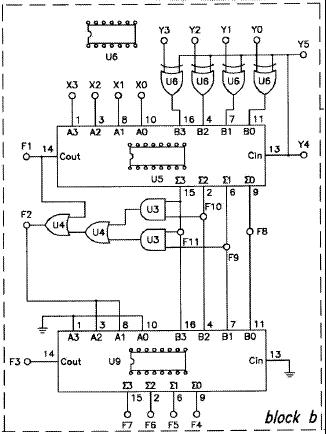
1. **Constructing BCD Adder** 
   1. Set the KL-26002 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block b.** The circuit, shown in **Fig1.12**, will act as a BCD adder.

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1. Connect inputs X0~X3 to SW0~SW3, Y0~Y3 to SW4~SW7, Y5 to ground (“0”).

**U5** and **U9** are 7483 4-bit binary full adder, connect outputsF8~F11 of **U5** to the inputs of one of the digital displays. F8~F11 should also be connected to Logic Indicators L1~L4. Connect F1 and F2 to logic Indicators L5 and L6, respectively.

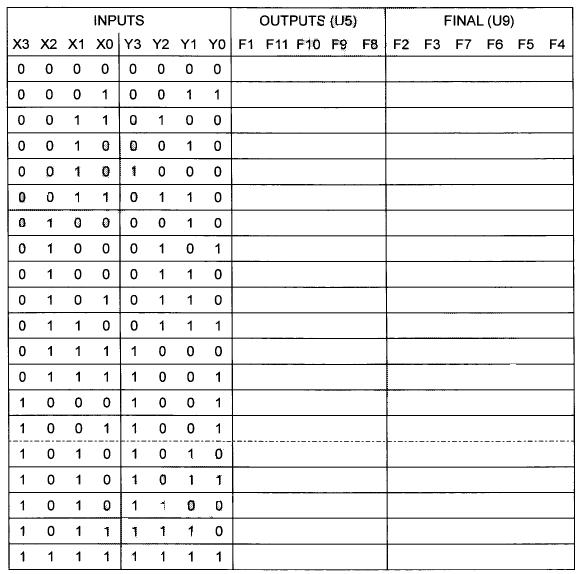
Connect outputs F4~F7 of U9 to inputs of another Digital Display. Also connect F4~F7 to L0~L3 and F3 to L4.



**FIG1.12: Wiring Diagram (KL-26002 block b)**

1. F11~F8 are the sum of X0~X3 added to Y0~Y3 while F1 is the carry. Follow the input sequences for X0~X3 and Y0~Y3 in the **table 1.7** and record the output state.

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**Table1.7**

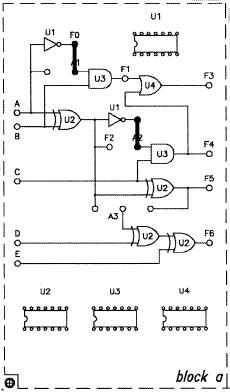
1. **Half- and Full Subtractor Circuits.** 
   1. **Constructing Half-/Full Subtractors with basic logic Gates.**

Design the Logic Diagram, Boolean function, and truth table of a half- and full- Subtractor**. (Pre lab)**

* + 1. Set the KL-26002 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block a. Complete the connections by referring to the wiring diagram in **Fig1.13**. Apply +5VDC from Fixed Power on KL-22001 Lab to KL-26002 Module.

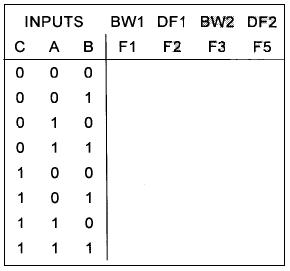
15

1. Connect inputs A~C to Data Switches SW0~SW2; outputs F2 to L1; F1 to L2; F3 to L3; F5 to L4. When C=0 the circuit is half-subtractor with the borrow output F1 (BW1) and the differences output F2 (DF1). When C=1 the circuit is a full-subtractor with borrow output F3 (BW2) and the differences output F5 (DF2).



**FIG1.13: Wiring Diagram (KL-26002 block a)**

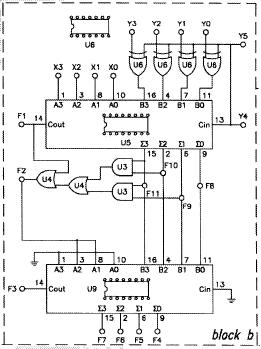
3. Follow the input sequences in **Table 1.9** and record output states.



**Table1.9**

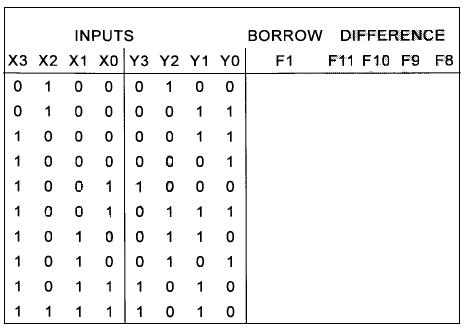
16

1. **Constructing 4-Bit Full-Subtractor with IC** 
   1. Set the KL-26002 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block b**. Apply +5VDC from the Fixed Power on KL-22001 lab to KL-26002 Module.



**FIG1.14: Wiring Diagram (KL-26002 block b)**

1. Connect inputs X3~X0 to SW7~SW4; Y3~Y0 to SW3~SW0. Connect outputs F1 to L1; F8~F11 to L5~L2. To execute the subtract operation, connect Y5 to +5V (“1”) (or Cin of U5=1). Follow the input sequences and record the output states in **Table 1.10.**



**Table 1.10**

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1. **Problem: Building Comparator Circuit**

A 4-input, 3-output circuit that compares 2-bit unsigned numbers and output a ‘1’ on one of three output lines according to whether the first number is greater than, equal to, or less than the other number. You can only use two 4×1 multiplexers.

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