BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Department of Electrical and Computer Engineering

Course Information	
Course Title	**Digital Electronics and Computer Organization Lab**
Course Number	ENCS 211
Semester	Scond Semester 2020/2021
Class Times	As per schedule, in Room: Masri107 or Online
Instructors/TAs	• Please consult Ritaj for Instructors, TAs and their office hours and office locations. Please check Ritaj regularly for messages on the course and experiments.
Office Hours	Please check Ritaj for the office hours of your instructor and TA

Course Objectives

- To become familiar with basic logic gates and using them to implement digital circuits.
- To study and implement combinational circuits (comparators, adders, decoders…)
- To study and implement sequential circuits (flip-flops, registers, counters…)
- To practice Verilog HDL and Quartus software.
- To become familiar with FPGA programming.
- To implement real FPGA based applications.
- To become familiar with main components and techniques used in computer systems such as ALU, main registers, instruction cycle…
- To became familiar with assembly programming and "Debug" program

ABET OUTCOMES

B: Ability to design and conduct experiments, analyze and interpret data,

C: Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, sustainability political, ethical, health and safety, manufacturability, and

K: Ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

Assessment Policy (may be revised based on delivery methods)		
Assessment Type	**Details**	**Weight**
Work Groups	• Normally, maximum of 3 students can work together in the Lab. For COVID 19 distancing may result in smaller teams or students working individually. Online sessions are individual.	
Reports	• 5 reports, written individually (one per student, not group). See outline for experiments with a report. • The report includes the pre-lab and the post-lab homework.	30%
Quizzes/ToDos	• In or after lab.	15%
Performance/Discussions/Homework	• Your performance will be monitored during the lab, and your results may be discussed after the lab. • Post-lab homework will be required in case the report is not required. • Attendance and being on time	15%
Final Exam: Theoretical	Testing digital foundations relevant to lab work. Date to be announced later.	15%
Final Exam: Practical, may include a project.	In lab experiment including wiring and Verilog implementations. Dates to be announced later.	25%

Tentative Schedule			
Meeting #	**Experiment**	**Report required?**	**Online/ InLab**
1	Experiment 1: Combinational Logic Circuits	No	**Online**
2	Experiment 2: Comparators, Adders and Subtractors	**Yes**	**Online**
3	Experiment 3: Encoders, Decoders, Multiplexers and Demultiplexers	**Yes**	**InLab**
4	Experiment 4: Digital Circuit Implementations Using Breadboard	No	**InLab**
5	***Experiment 8: Introduction to Quartus Software***[1]	**Yes**	**Online**
6	Experiment 5: Sequential Logic Circuits	**Yes**	**Online**
7	Experiment 6: Sequential Logic Circuits using breadboard and Integrated Circuits	No	**InLab**
8	Experiment 7: Constructing Memory Circuits Using Flip-Flops	**Yes**	**Online**

[1] Please make sure to install quartus software on your laptop in time for this experiment. E.g. the following link (more later) http://www.mediafire.com/file/eqd7xidoan3exqv/90_quartus_free.exe

9	Experiment 11: Arithmetic Elements	No	**Online**
10	Experiment 9: A Simple Security System Using FPGA	No	**InLab**
11	Experiment 10: Simple Computer Simulation Using FPGA	No	**Online**
12	Make-up session		
13	Practical Final exam		**InLab**

The **InLab** **sessions will be done at least two experiments a day (Saturdays/Sundays). The schedule will be communicated to you later.**

Report Format

5 reports are required from each student (see the table above). The report is individual and the report mark will only be given to one student.

Your report must include:

Content	Points
Cover letter	1
Objectives	1
Brief theoretical review	2
Prelab	2
All experimental results and circuit schematics.	3
Solutions for tasks involved	3
Discussion and Evaluation	3
Conclusions	2
Figure and page numbering, Text size and references	2
Time took you to do the experiment (in lab) and feedback about the experiment	1
Total points	20

Simulators:

Proteus Simulator: https://www.labcenter.com/
(more on installation later).

ميثاق شرف الأمانة الأكاديمية

بموجب التسجيل في هذا المساق يلتزم الطالب باحترام أنظمة وقوانين الجامعة وخاصة تلك المتعلقة بالأمانة العلمية وعدم الغش. ويتحمل الطالب مسئولية ذاتية، أدبية وقانونية، عن المحافظة على الأمانة العلمية وذلك بالامتناع عن الغش في الامتحانات والوظائف والتقارير، وعدم السماح لغيره من الطلاب بأن ينقلوا عنه في الامتحانات والوظائف والتقارير.

يستوجب الغش أو محاولة الغش التوبيخ والإجراءات القانونية المنصوص عليها في تعليمات الأمانة الأكاديمية التي أقرها مجلس الجامعة، وتشمل ما يلي:

1. **العقوبة الأكاديمية: يقررها مدرس المساق وقد تصل إلى علامة رسوب في المساق.**
2. **العقوبة التأديبية: تقررها لجنة النظام في الكلية وقد تصل إلى الفصل المؤقت أو النهائي من الجامعة.**

بموجب تسجيلي في هذا المساق واستلامي لهذا الميثاق أتعهد أمام الله أن أحافظ على الأمانة الأكاديمية بأن أمتنع عن الغش، وأن لا أتسامح مع أي محاولة للغش من قِبل الآخرين.