Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Systems “ENCS234”

Introduction to Quartus II

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➢ Objective

- ❖ Download Quartus II software tool.
- ❖ Create a simple task to take an idea how to use Quartus II software tool.

➢ Introduction

The Altera Quartus II software tool is an available environment for System on Programmable Chip design. This tutorial is not intended to be an exhaustive reference manual for the Quartus II software. Instead, it is a guide that explains how to install Quartus II software tool, build a project, compile a created project and then simulate it.

Table of Contents

1 How to Download Quartus II

Open the following link to Download Quartus II

- Link:

http://www.mediafire.com/file/eqd7xidoan3exqv/90_quartus_free.exe/file?fbclid=IwAR0Mmufw-YBRjv4l7uGM9l_6V_5WKokZ20z_lTPc9QJrNsL92IkrzMB-h8A

Follow up the following 16 Figures

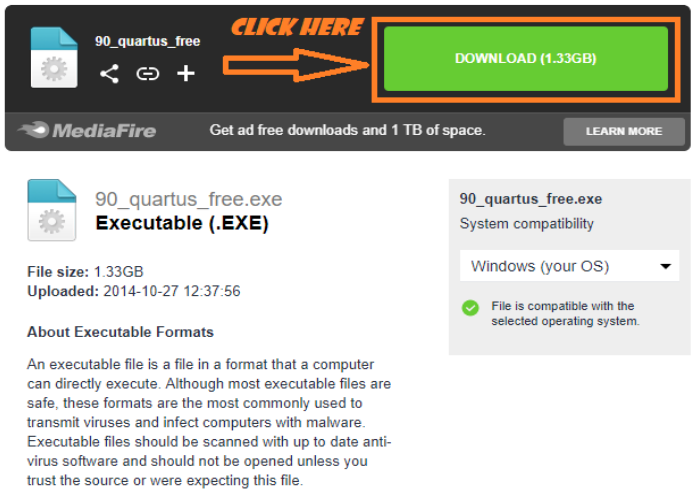


Figure 1.1: After Opening the Link.

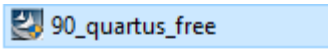


Figure 1.2: setup file, open it.

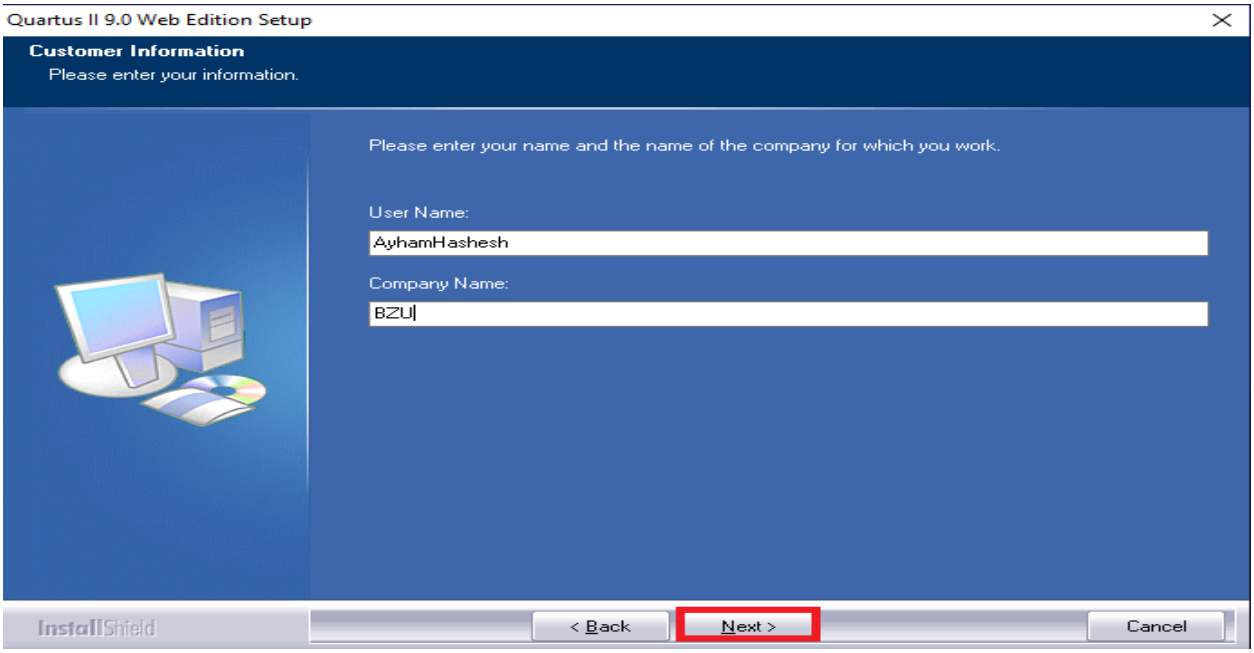


Figure 1.3: Fill yourname and company name as shown.

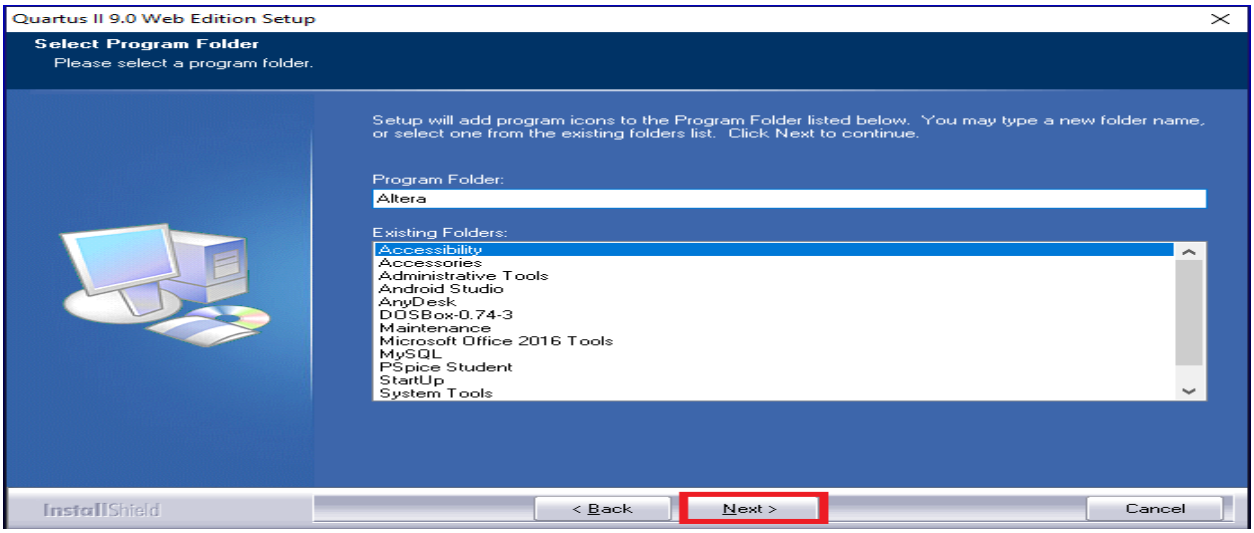


Figure 1.4: Select Accessibility then click next.

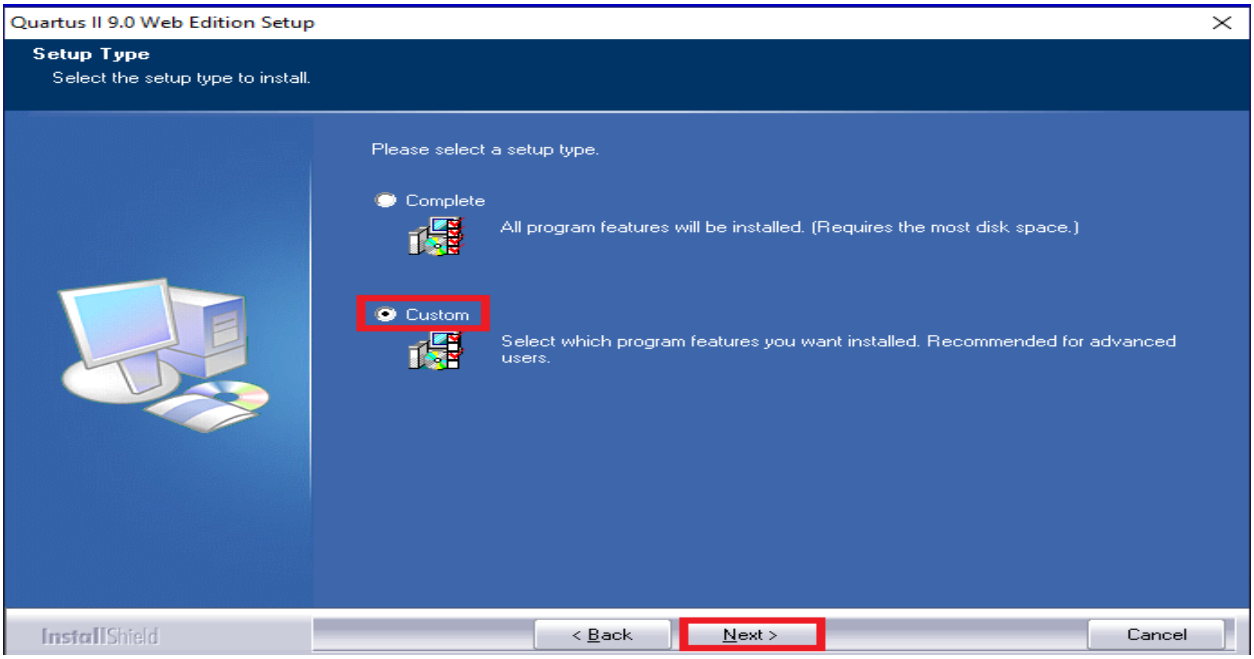


Figure 1.5: Select custom then click next.

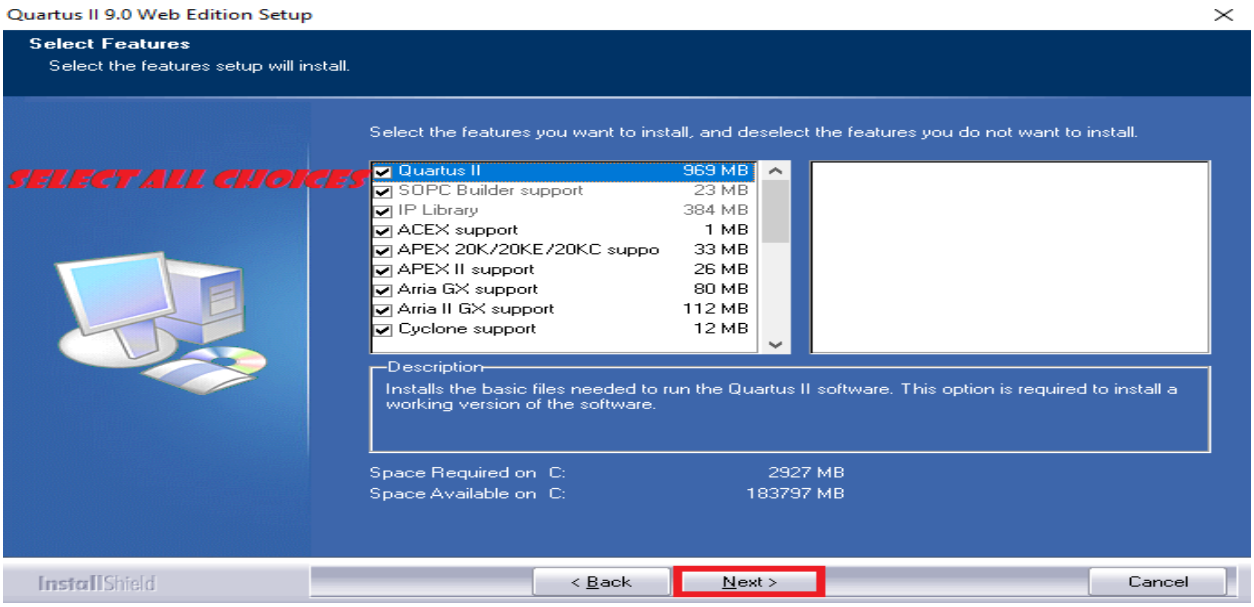


Figure 1.6: Select all choices.

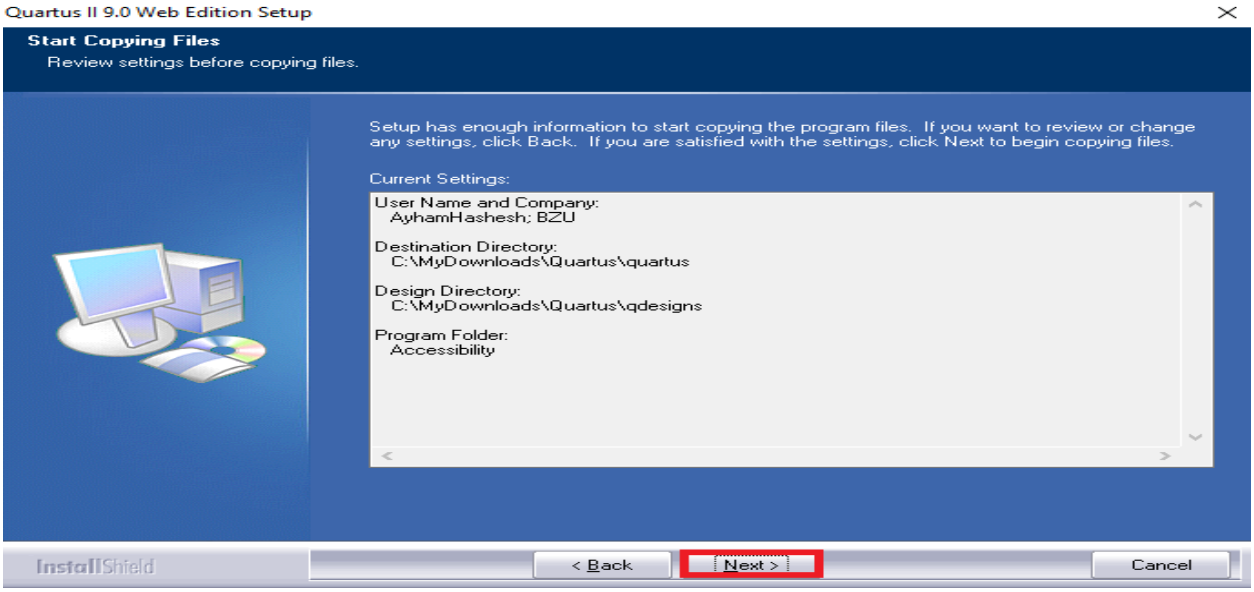


Figure 1.7: Select next.

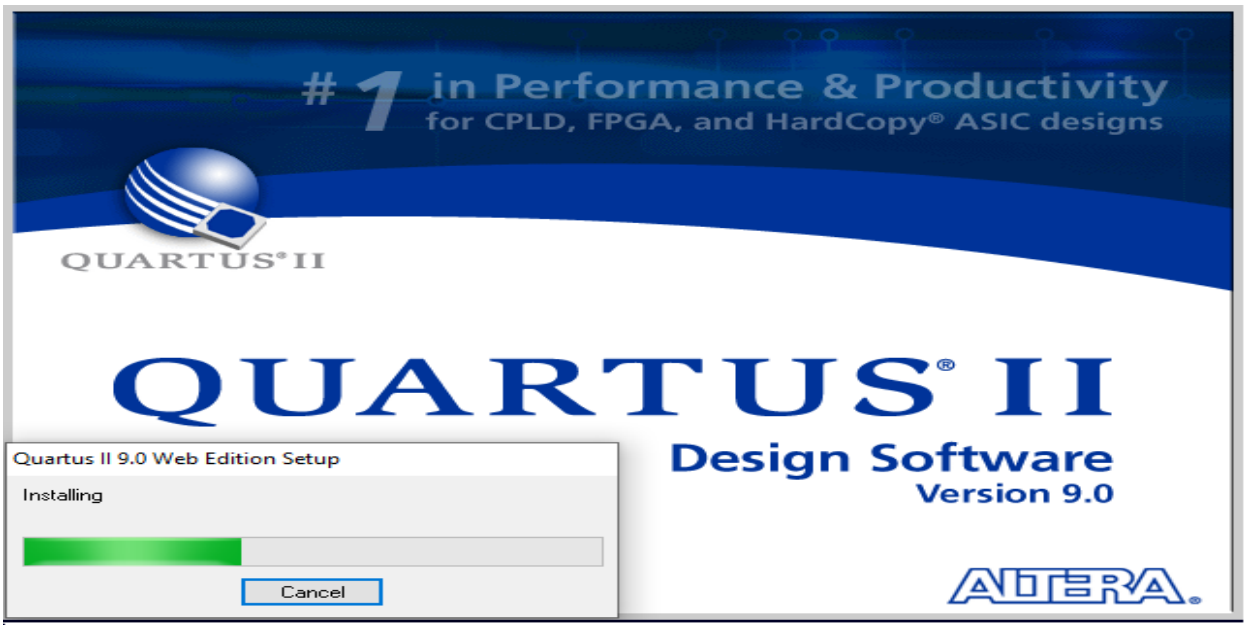


Figure 1.8: Wait it until it finished.

Figure 1.9: To create a shortcut on the Desktop.

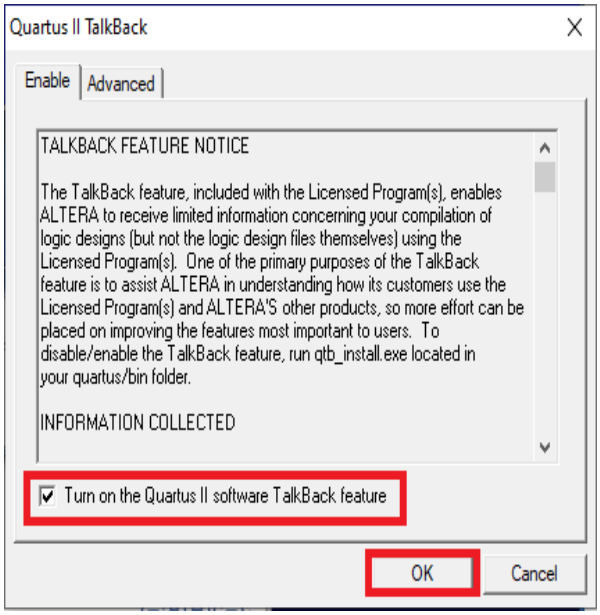


Figure 1.10: Select as shown.

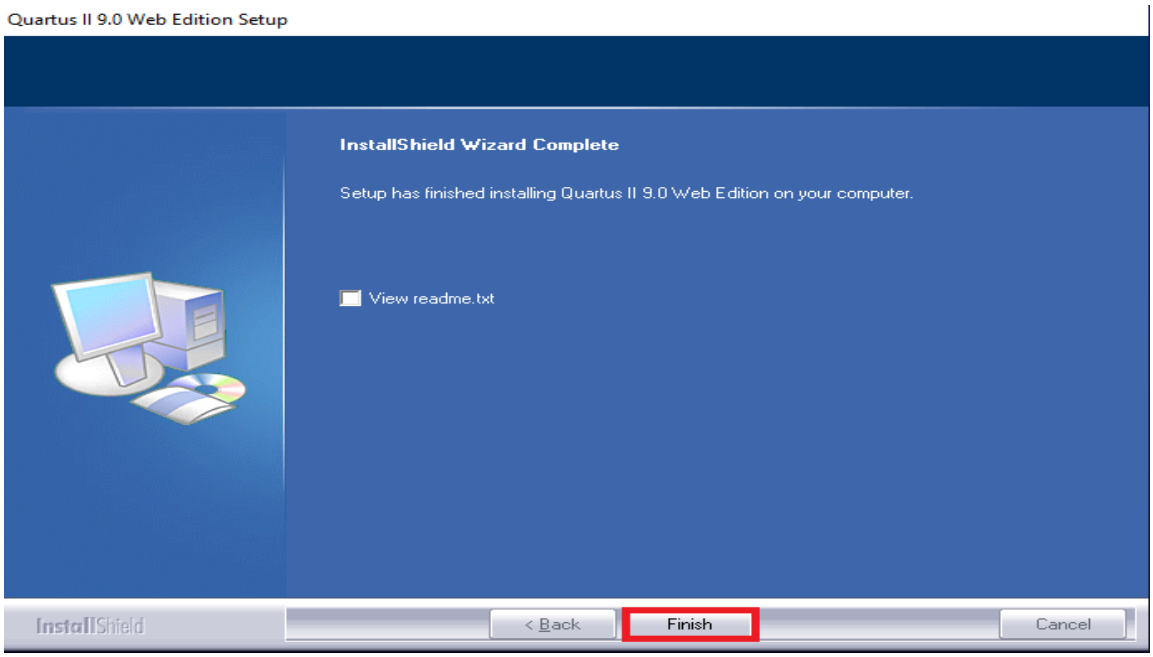


Figure 1.11: Select Finish.

Figure 1.12: Open it.

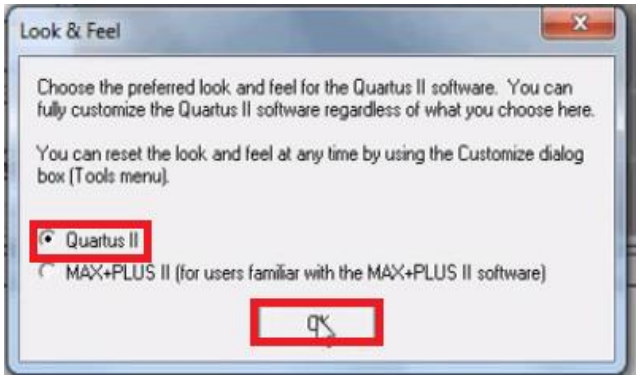


Figure 1.13: Select as shown.

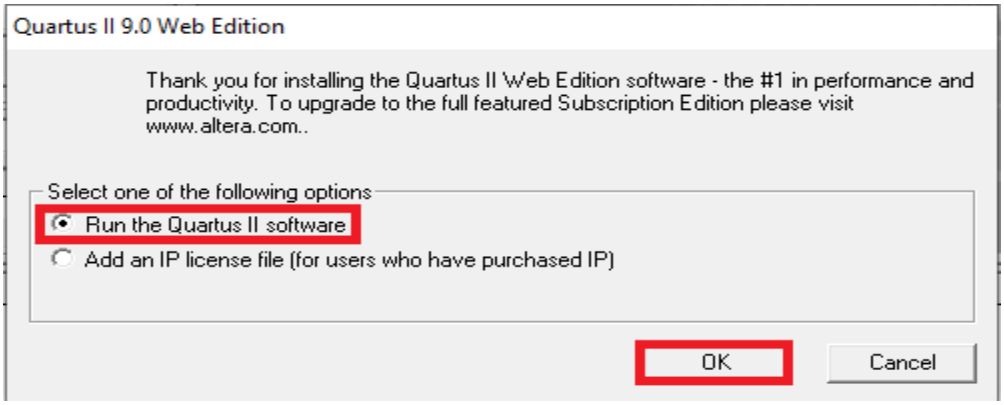


Figure 1.14: Select as shown.

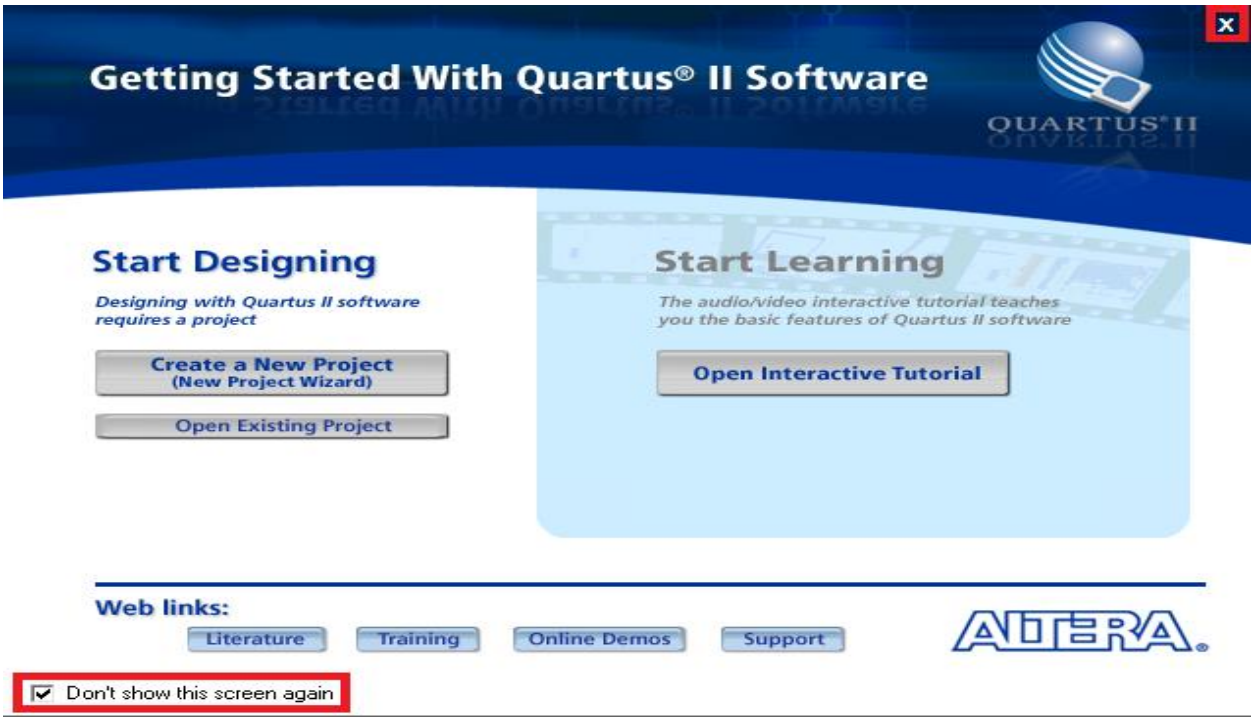


Figure 1.15: Select as shown.

Finally, you will have as shown in Figure 1.16

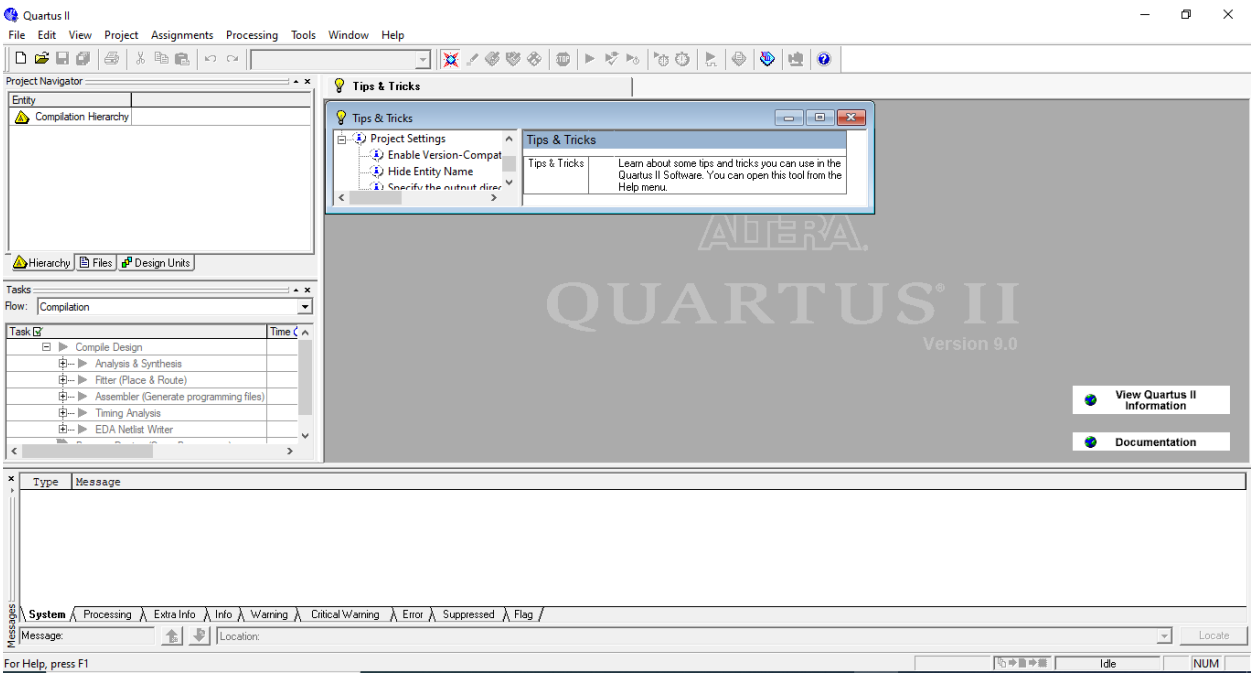


Figure 1.16

Now, we will take a simple task to take an idea about the software tool (Quartus II)

2 Task

By using the installed Quartus II software tool, make a design for Mux 2x1 the simulate it.

1 Project Creation

Select “File”, then click on “New Project Wizard” as shown in Figure 1.1, then follow up the following figures (Figure 1.2 – Figure1.12).

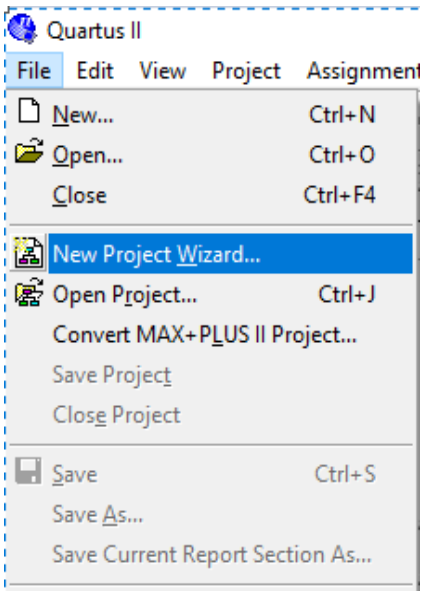


Figure 1.1

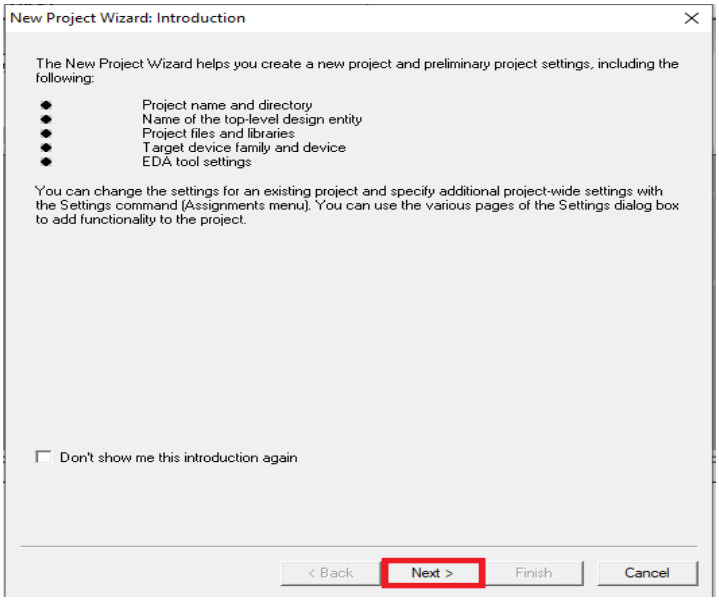


Figure 1.2

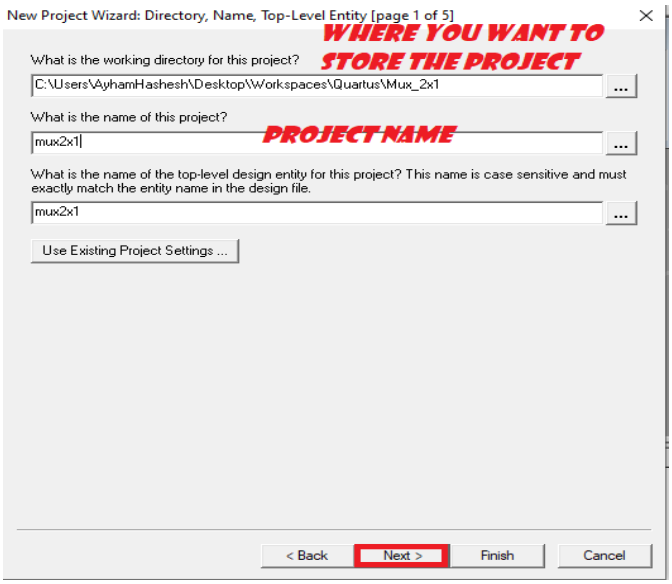


Figure 1.3

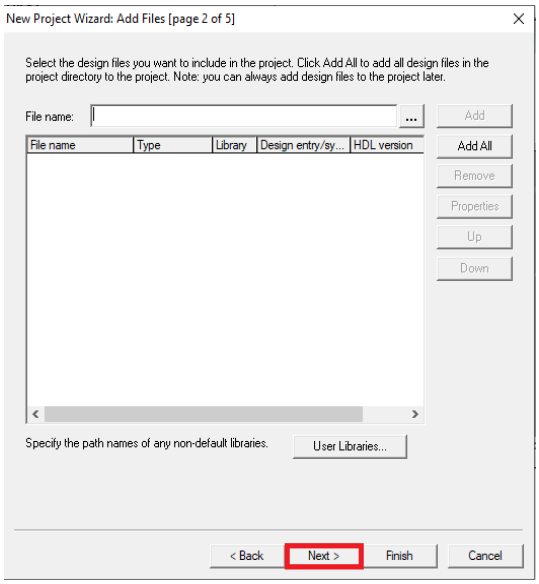


Figure 1.4

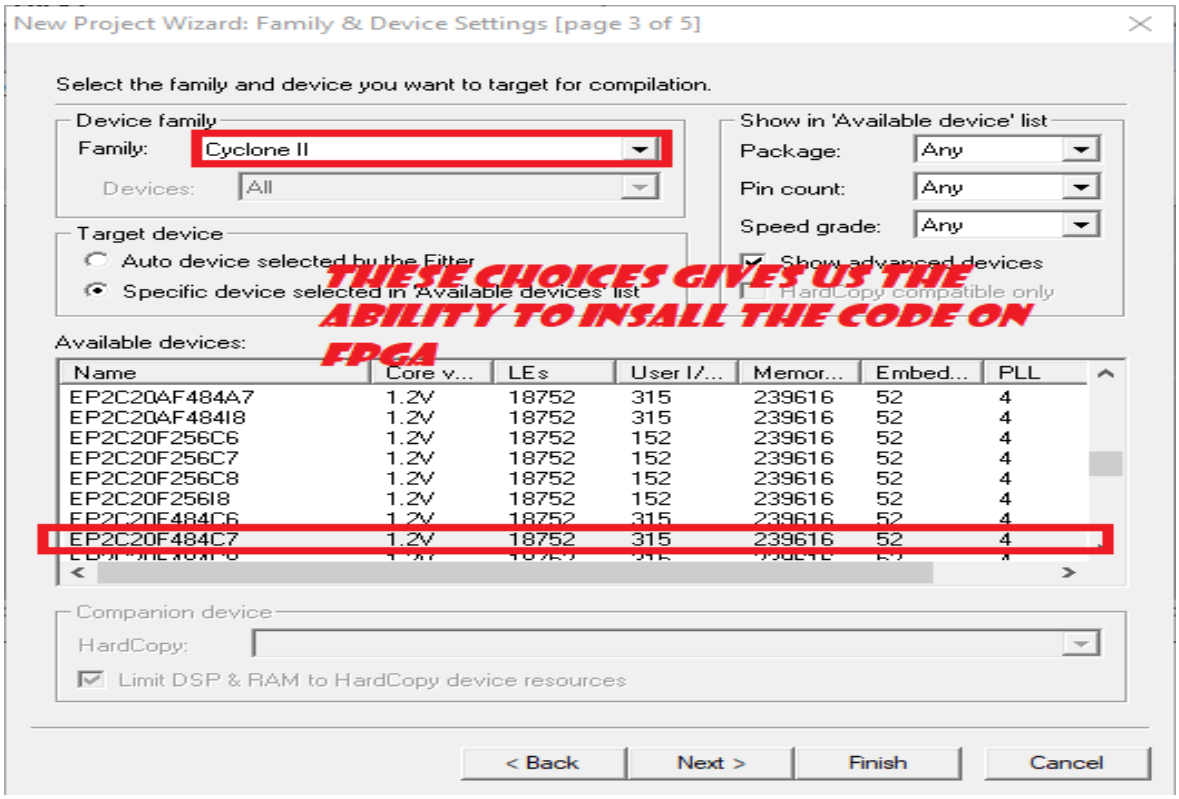


Figure 1.5

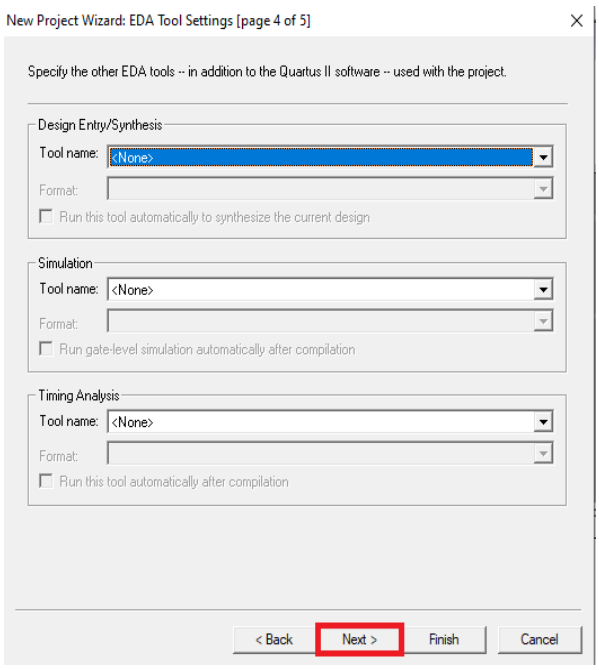


Figure 1.6

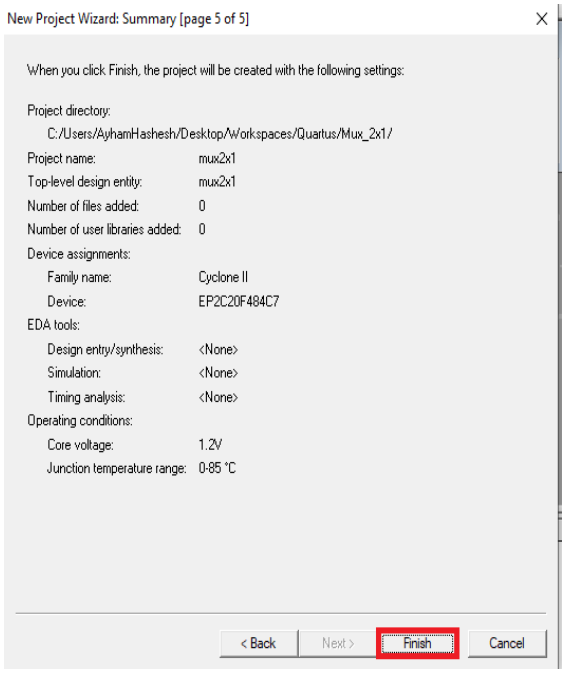


Figure 1.7

After the previous steps you will have as shown in Figure 1.8. If you select files you will find it empty.

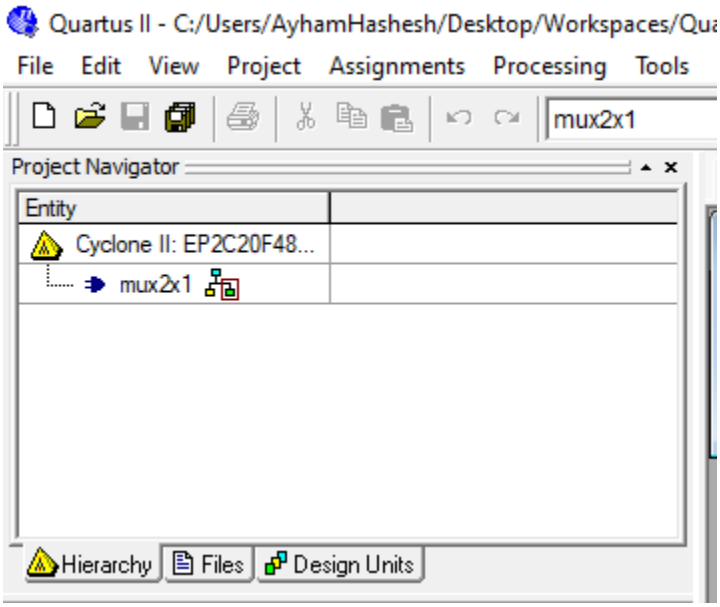


Figure 1.8

Let us create our files.

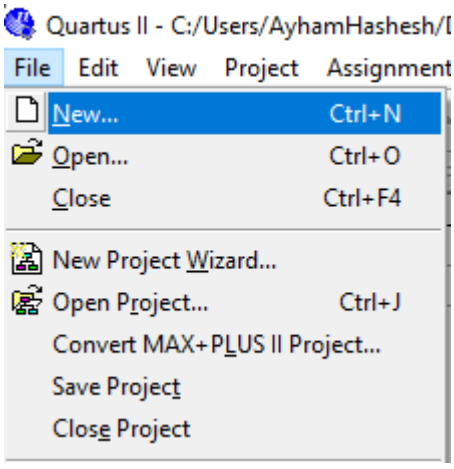


Figure 1.9

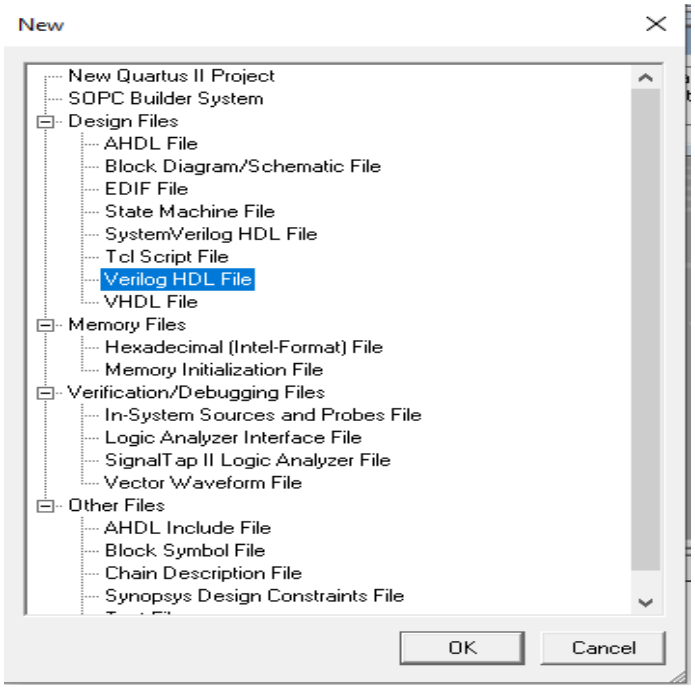


Figure 1.10: Select Verilog HDL File

Write your code in the appeared empty blank as shown in Figure 1.11

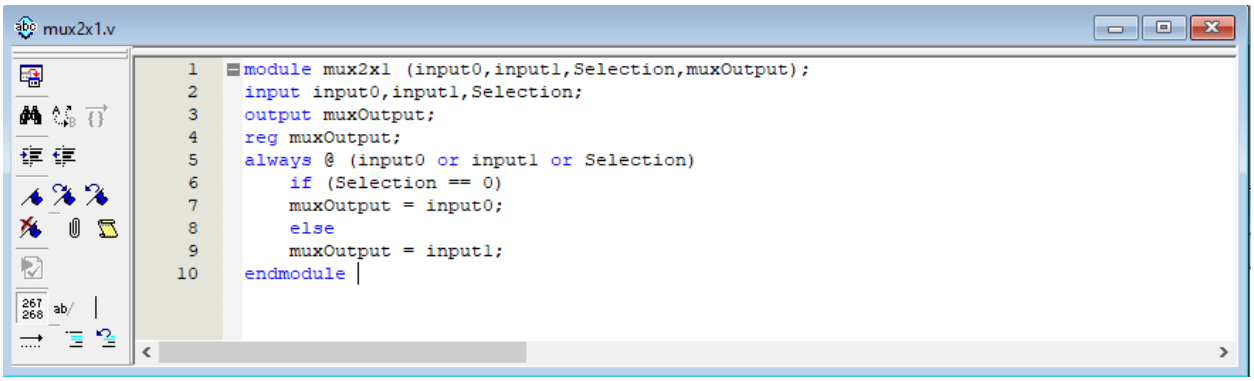


Figure 1.11: Write your code here

Important Notes

- The blue words like (module, input, etcetera …) are reserved words. Don't use these words as names for your variables.
- After write your code, press (Ctrl + S) to save it. **You have** to name the file as module name (in our case mux2x1), if you don't you code will not work.

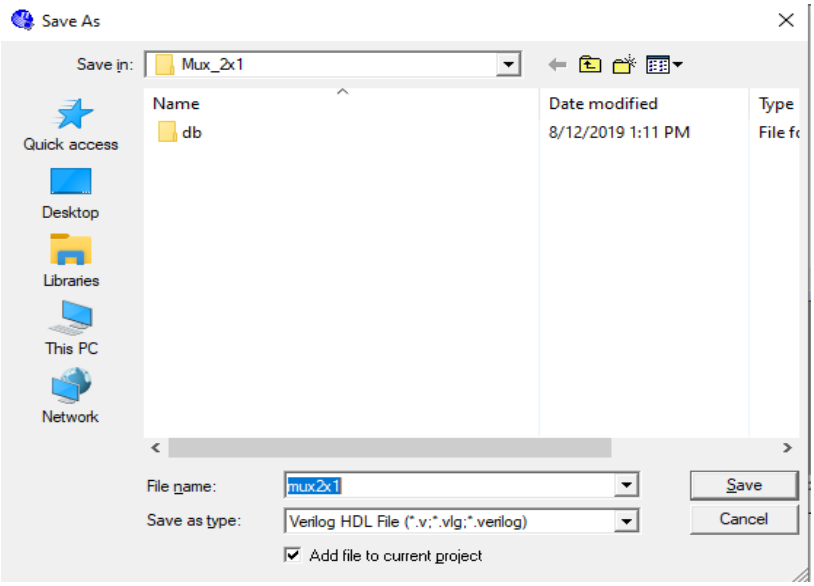


Figure 1.12: Name must be as module name

2 Compilation

Now, let us compile our project to check that there is no error. If you go back to Figure 1.8, you will find a change, your module has been created there. Right click on it then choose "Set as Top-Level Entity" as shown in Figure 2.1. then do as Figure 2.2

Important Notes

- Entity equivalent to module.
- This step to tell the Quartus which module to compile. Our project is simple but in complex projects many modules are exist. So, Quartus II can't decide by itself.

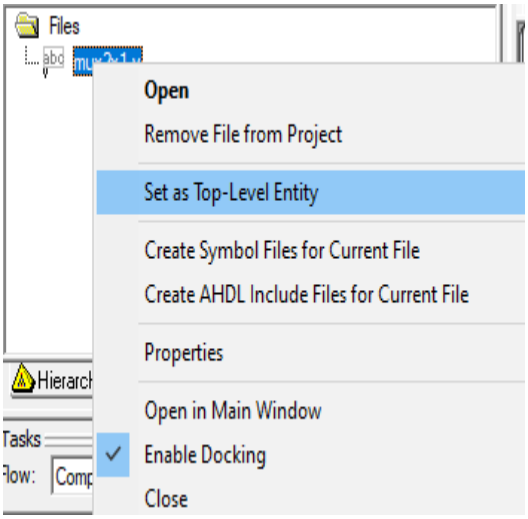


Figure 2.1: Select "Set as Top-Level Entity"

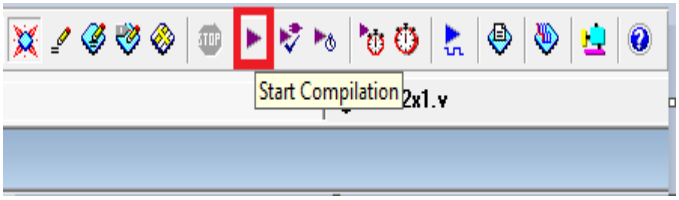


Figure 2.2: Select as shown to start compilation

After finsih you will have as shown in Figures (2.3 and 2.4). No need to worry about warnings)

If erroes are exist you will find them in the consule window.

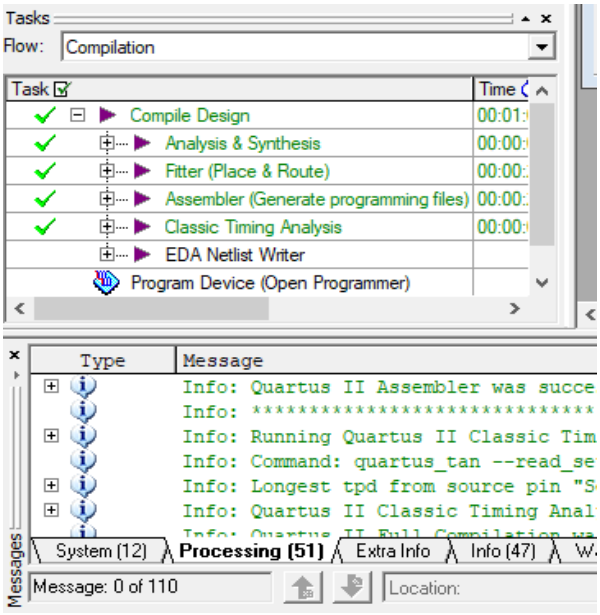


Figure 2.3

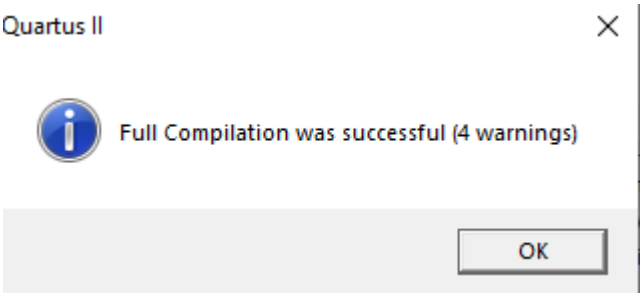


Figure 2.4: Click Ok.

Now, Let us simulate our code to compare the results with studied one (**Recall** Table 1.1)

Table 1.1: Mux 2x1 Truth Table

Selection	Input0	Input1	muxOutput
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

3 Simulation

Select “File” >> “New” >> “Vector Waveform File”. (see Figure 3.1)

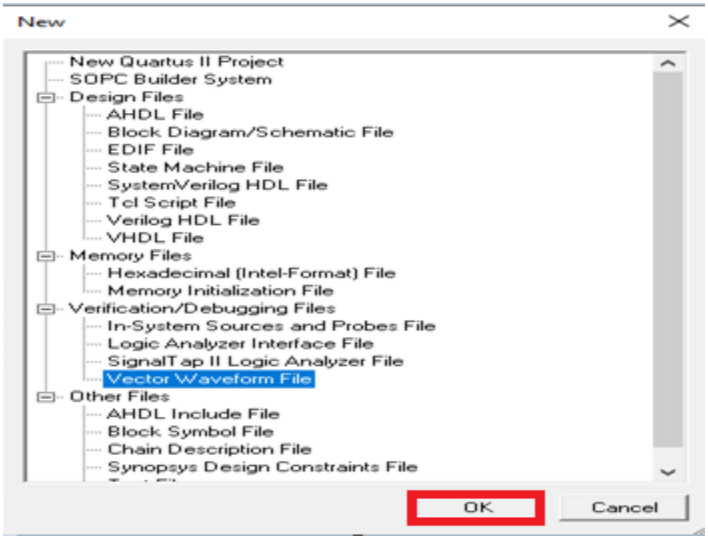


Figure 3.1

From the obtained empty blank, Right Click at the left side as shown in Figure 3.2

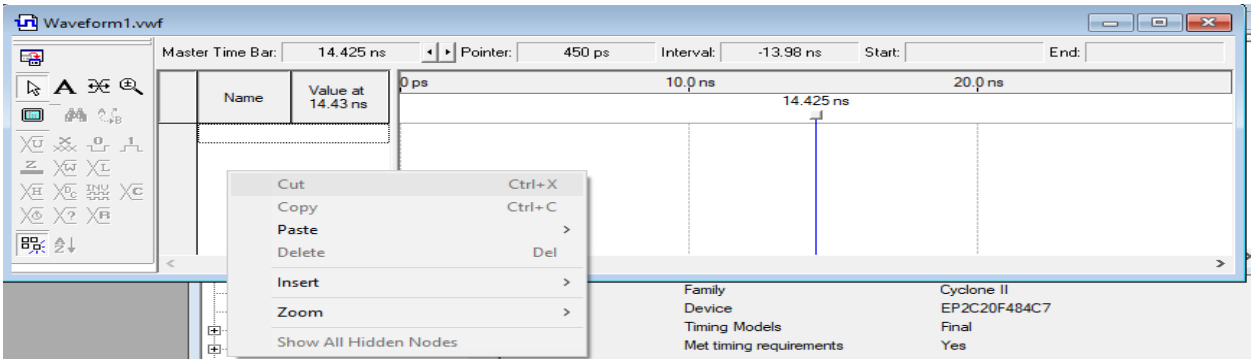


Figure 3.2

Select “insert” >> “insert node or bus …” >> you will obtained as Figure 3.3

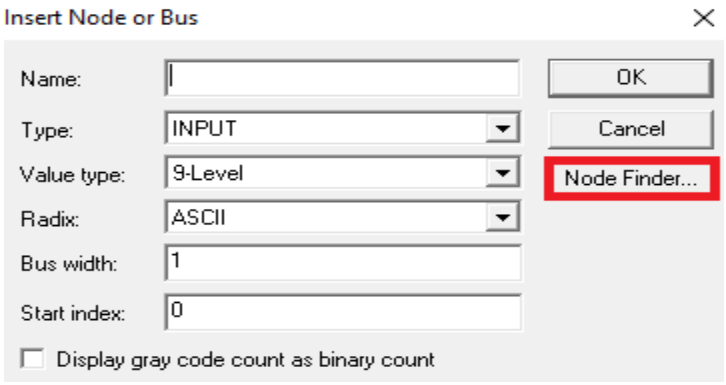


Figure 3.3: Select Node Finder

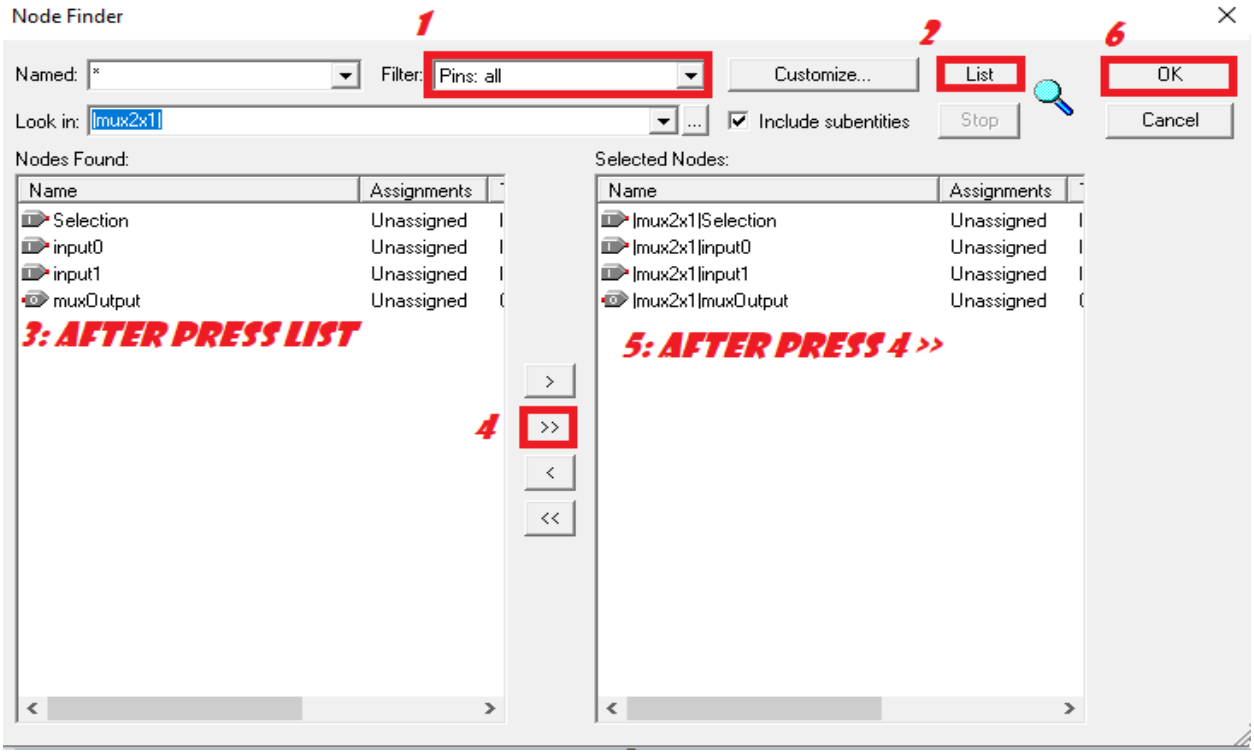


Figure 3.4: Follow the steps from 1 to 6

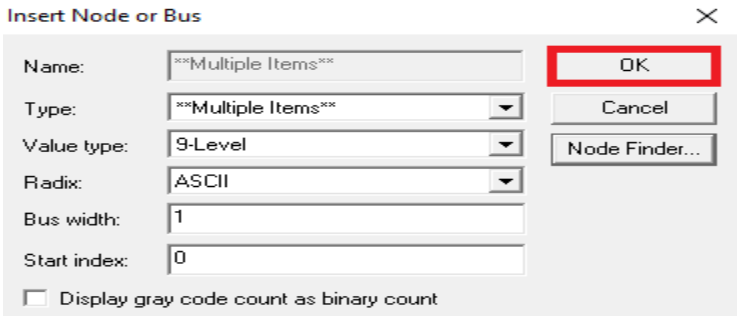


Figure 3.5: Press Ok

As we can see from Figure 3.6, the output are don’t cares at all the intervals.

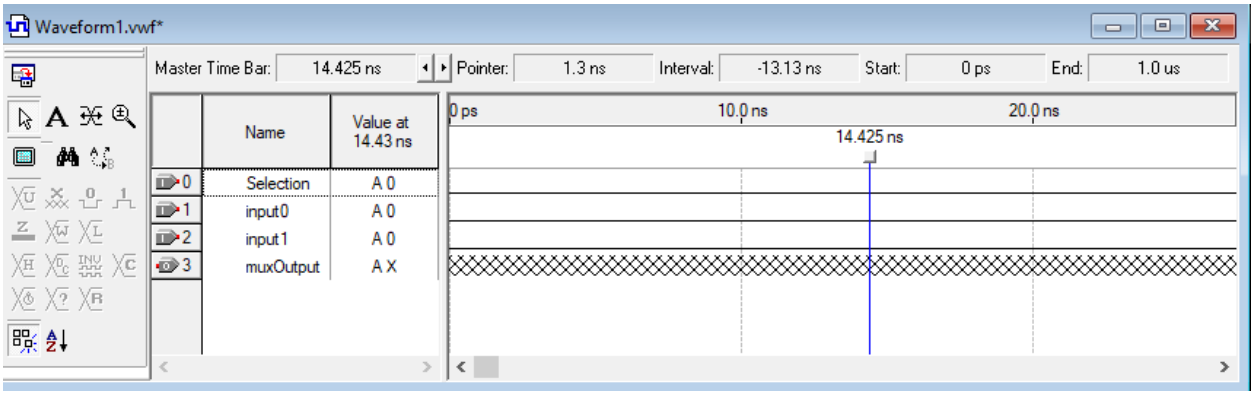


Figure 3.6

Now we have to set the interval that we want to see the output at it.

Figure 3.7 must be done for all inputs. (Selection, input0 and input1)

I have used 5ns, 10ns and 15ns consecutively

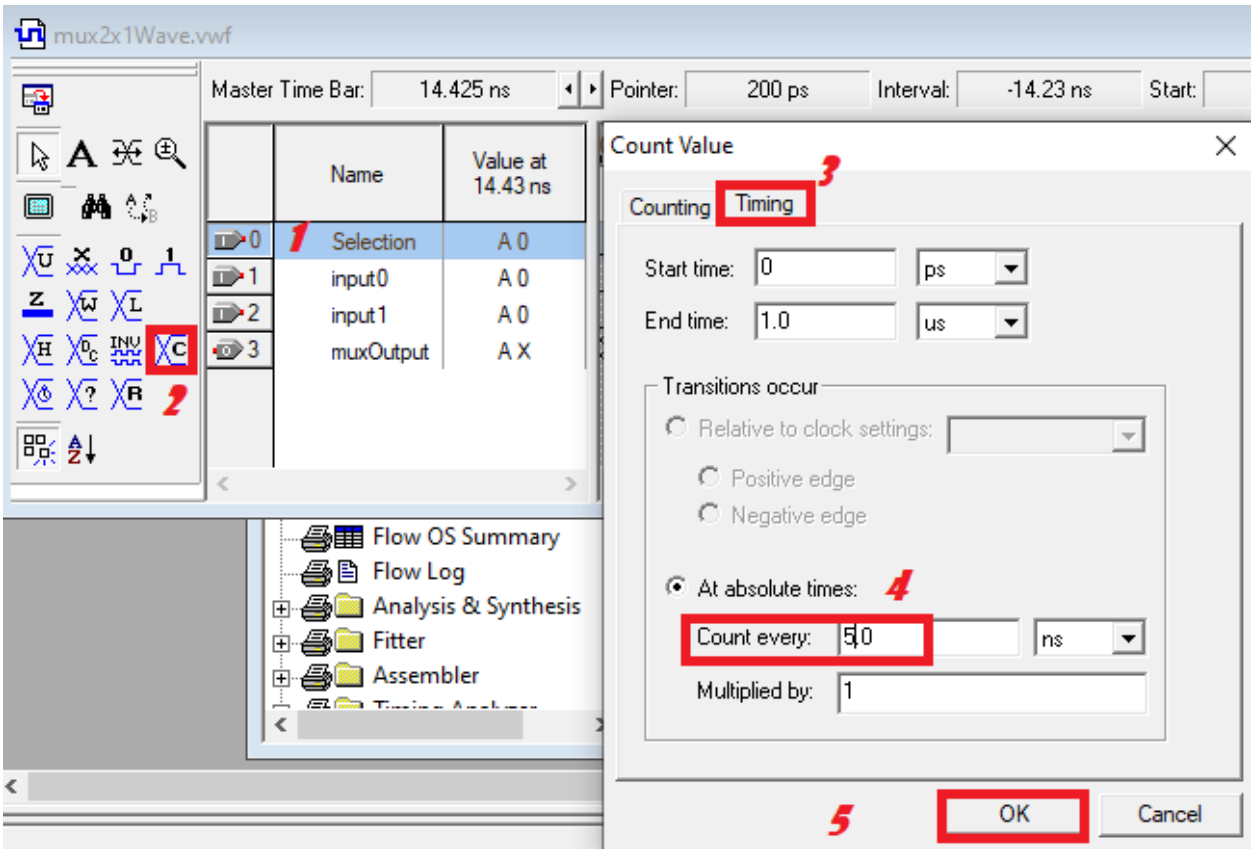


Figure 3.7: Must be done for all inputs.

After you finish you will have as shown in Figure 3.8. Output still Don’t cares.

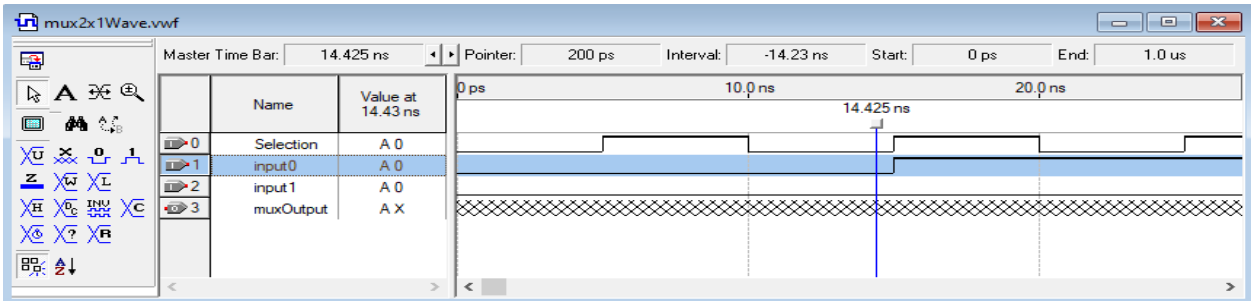


Figure 3.8

Before test our code press “ Ctrl + S” to save it (you can choose any name). See Figure 3.9

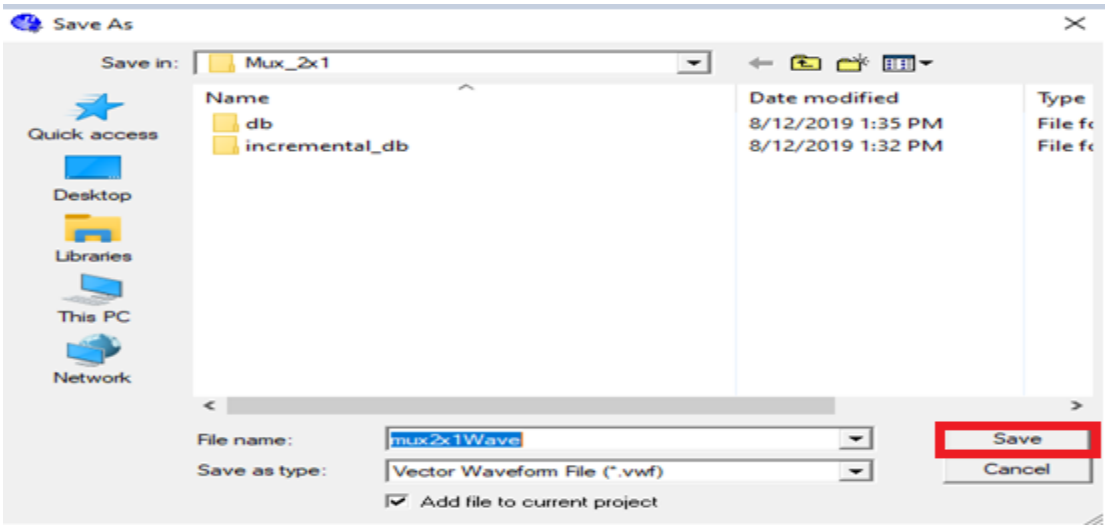


Figure 3.9

Select as shown in Figure 3.10

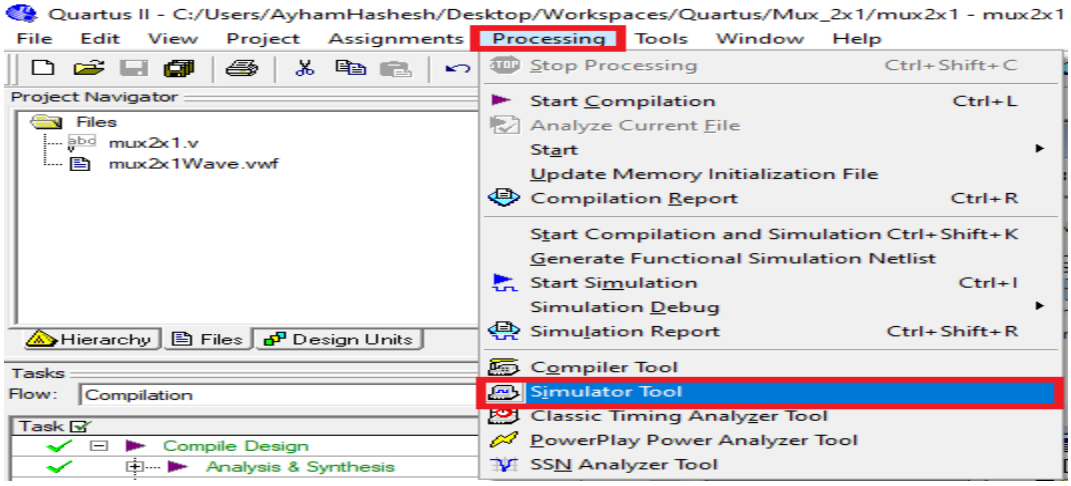


Figure 3.10

Follow Figure 3.11

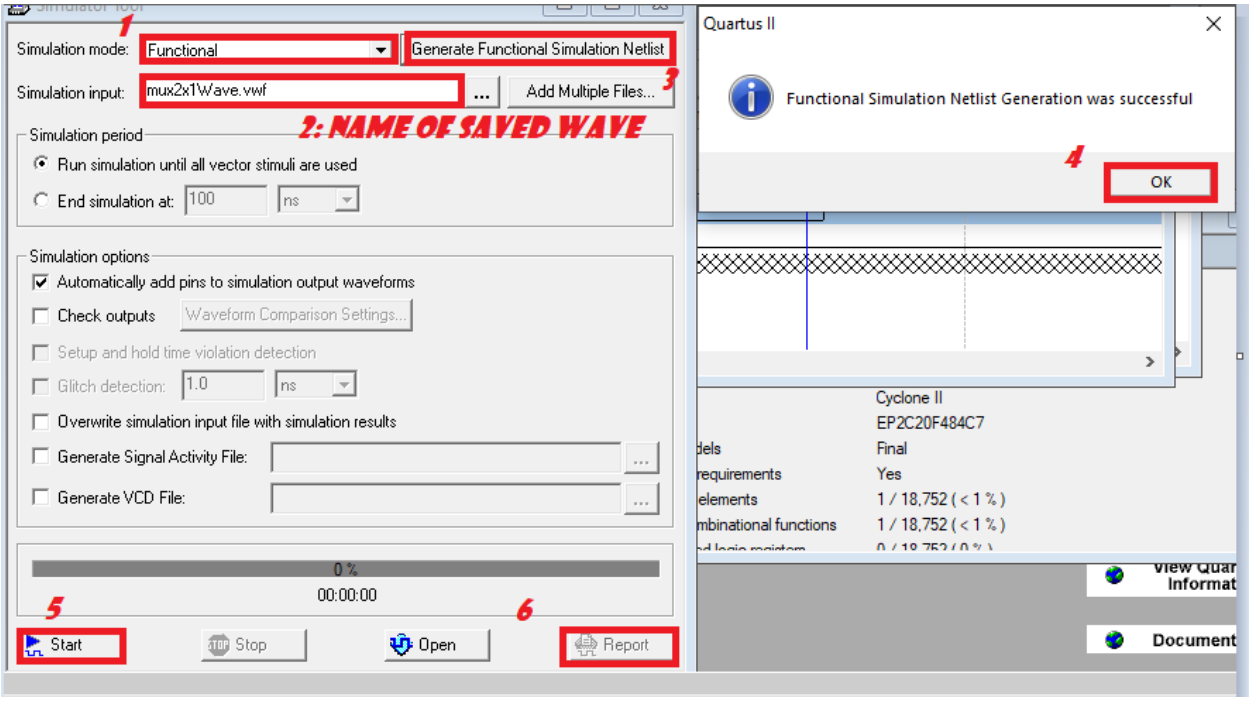


Figure 3.11: follow the steps from 1 to 5.

After Pressing Report, the results will be shown as Figure 3.12

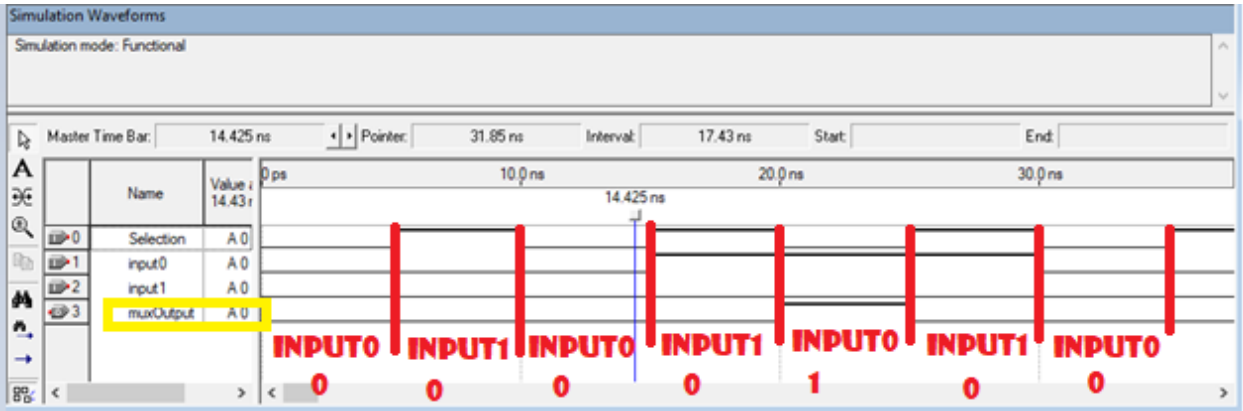
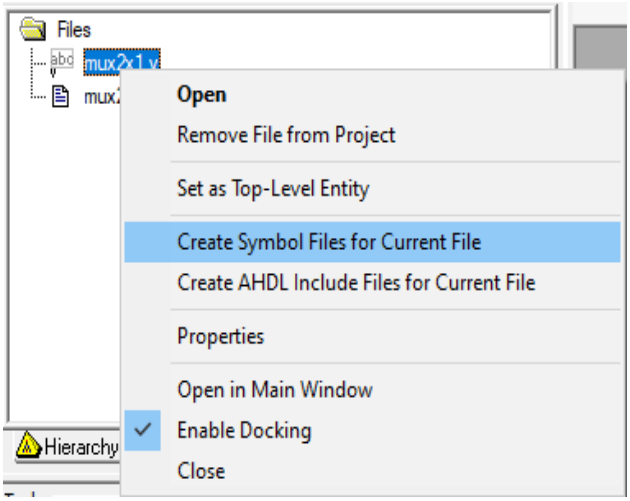


Figure 3.12

In the previous steps we can do the simulation for each component separately. But, in the real projects, there is more than one module. So, we will need something to make our design easier, this something called “Symbols”

4 Symbols Creations

Do as Figure 3.1. This symbol will be located in the memory to give us the ability to use it directly.



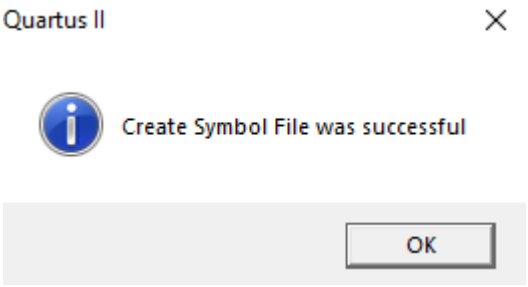


Figure 4.1" Create Symbol Files for Current File". *Figure 4.2*

Select "File" >> "new" >> "Block Diagram/Schematic File" (see Figure 3.3)

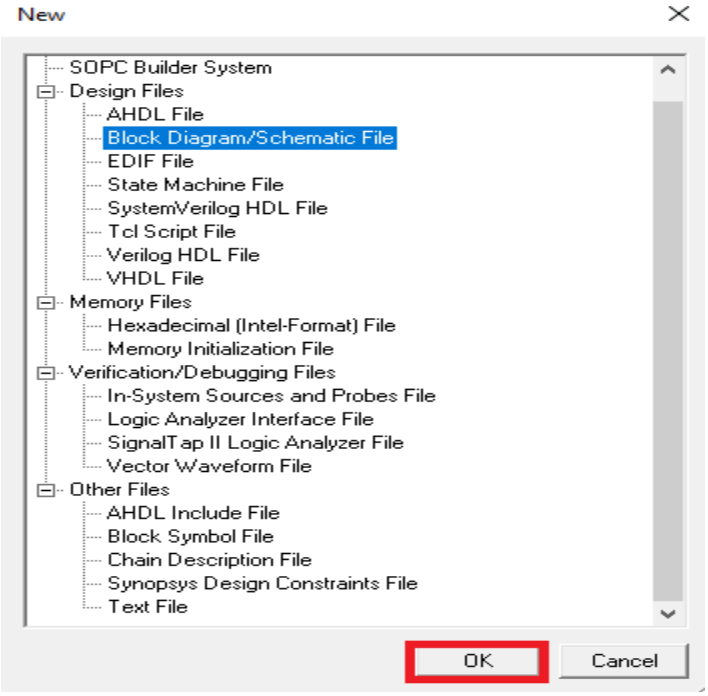


Figure 4.3: Select as shown.

An empty blank (1) will be shown, double click on it well show blank (2). See Figure 3.4

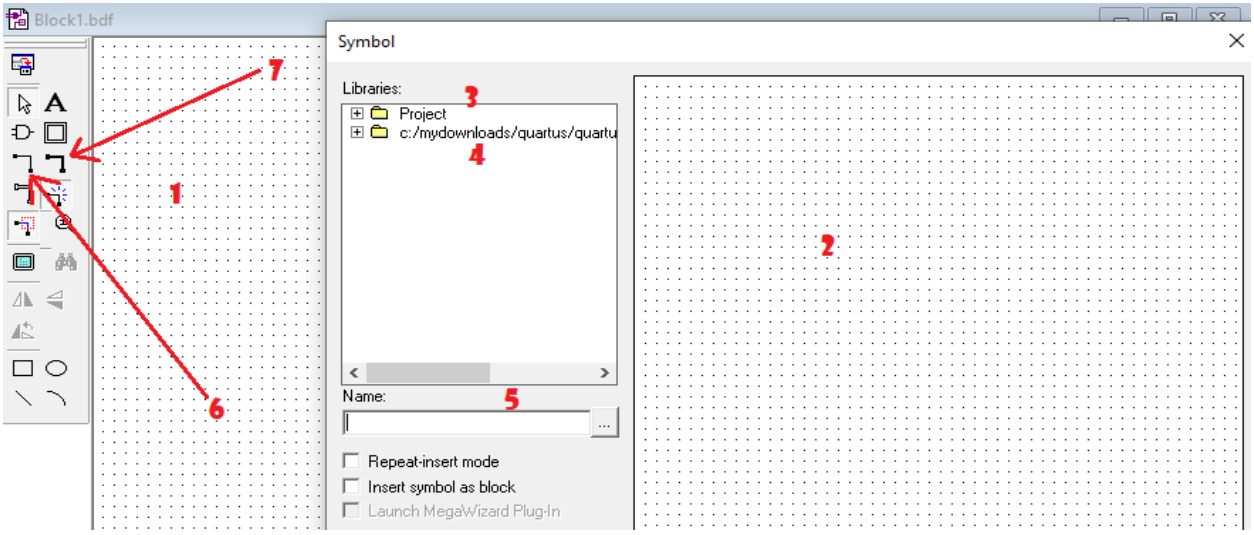


Figure 4.4

- ✓ **Note that**: We will add the created blocks from “Blank 2” to “Blank 1”.

From Figure 4.4

Number 3 (Project folder at the left side of blank 2)

contains our symbols (mux2x1 in our case).

Number 4 (the second folder) contains built-in modules like and gates, or gates, inputs and outputs ports and several useful components.

Number 5 used to search for components

Important Notes:

- Don’t miss use buses, and be careful when you connect them as they connected as you need and no node consist from the collision between them.
- **Number 6**: Orthogonal node tool: One Bus (we will use for individual inputs)
- **Number 7**: Orthogonal Bus tool: multiple Buses (used when declare arrays in module, you have to name each bus!)

Now try to build the Figure 3.5. you can Compile and Simulate it as shown previously.

- ✓ **Note that**: you can change the name of components by double clicking on it

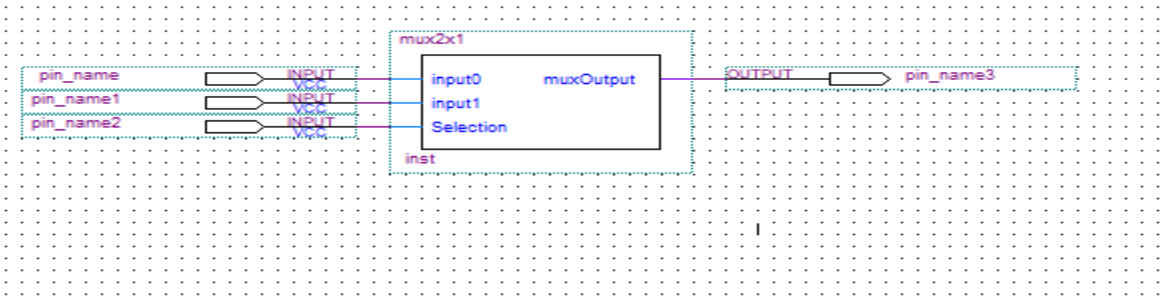


Figure 4.5: System Design