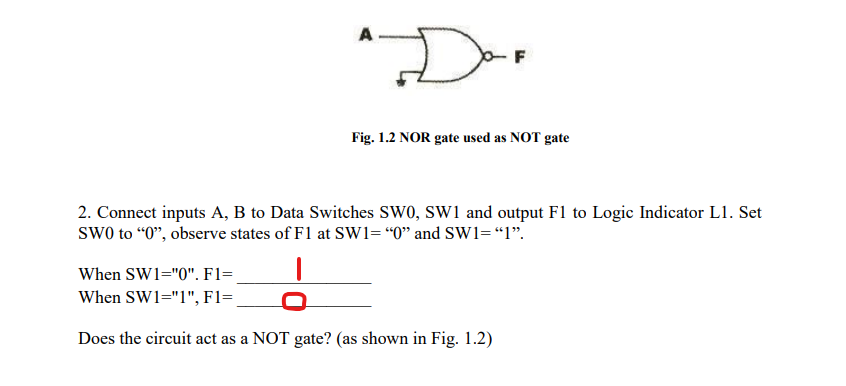
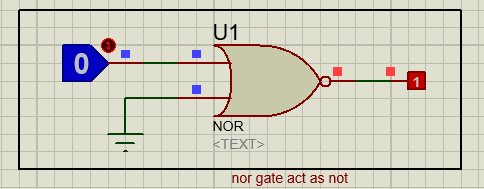
ISLAM JIHAD 1191375

Exp 1

 Yes it does



Here it depends on the input only because it’s an OR gate with not on the end that make the negative of it.

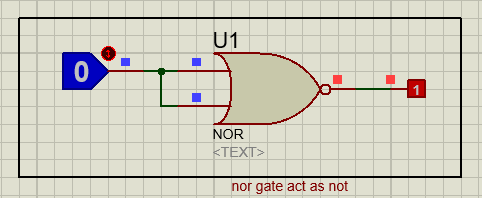
3. Insert a connection clip between A and B as shown in Fig. 1.3 below. Connect A to SW0 and F1 to L1. What is the state of F1 when SW0=0 and SW0=1?

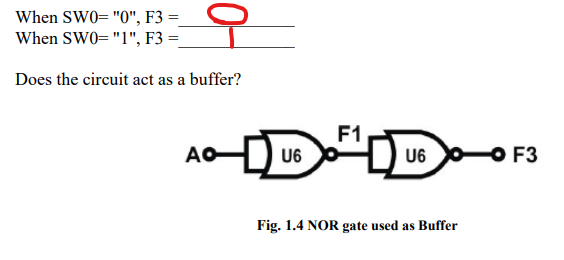
When SW0="0", F1= **1**

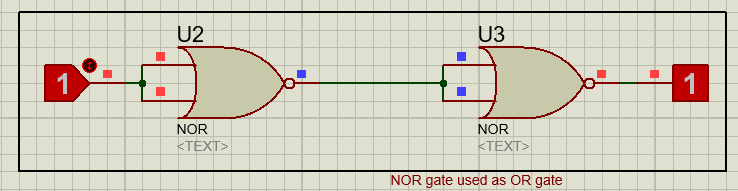
When SW0="1", F1= 0

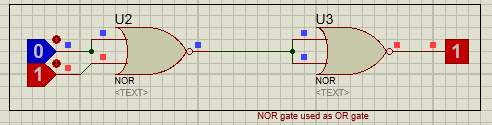
Does the circuit act as a NOT gate?

Yes

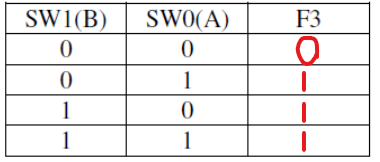


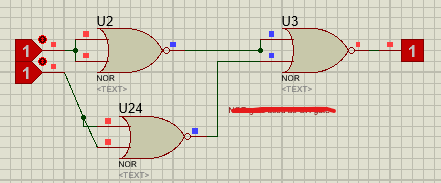


Yes it does

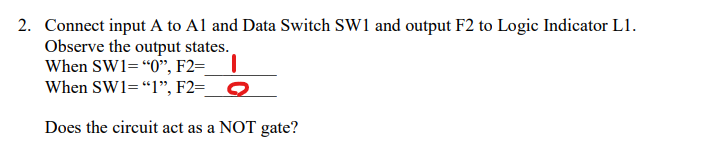


NOR gate used as OR gate, with one input and two

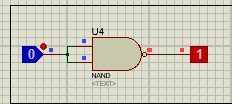


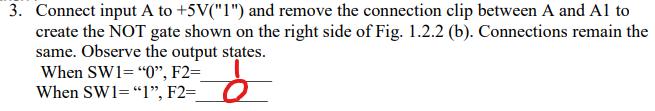


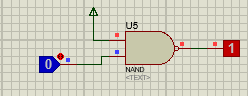


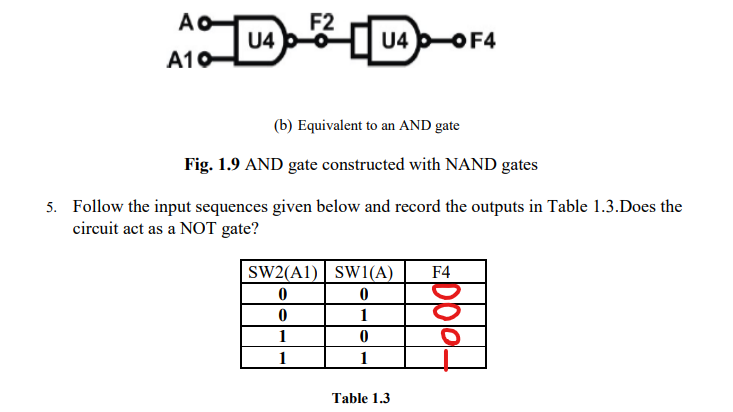


yes

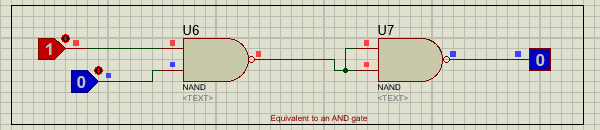




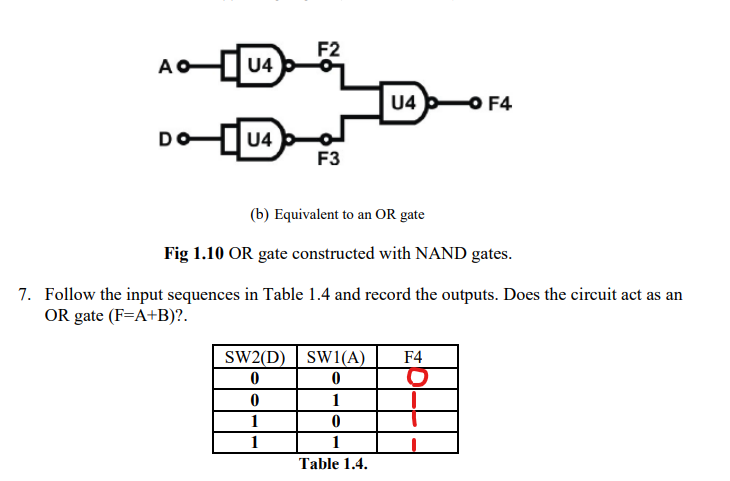




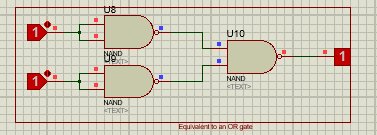
Yes it does

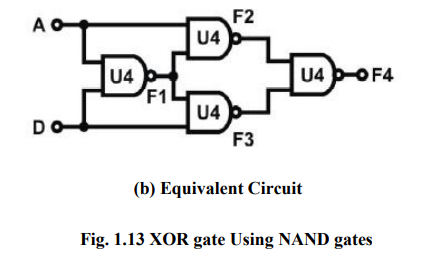


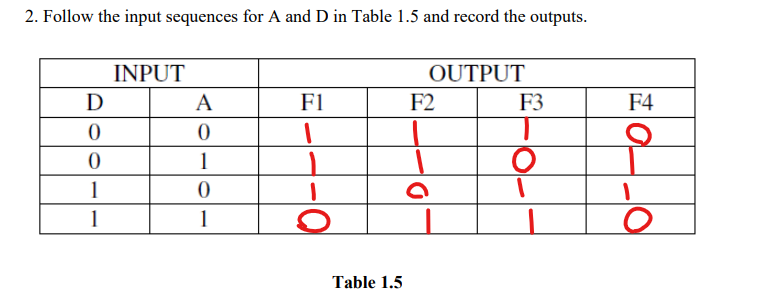
Here I made and gate using NAND gates, and it works the same as demorgan low (B’)’= B

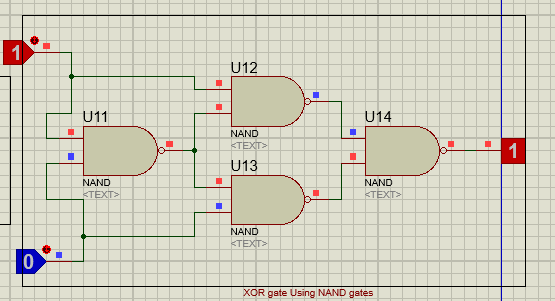


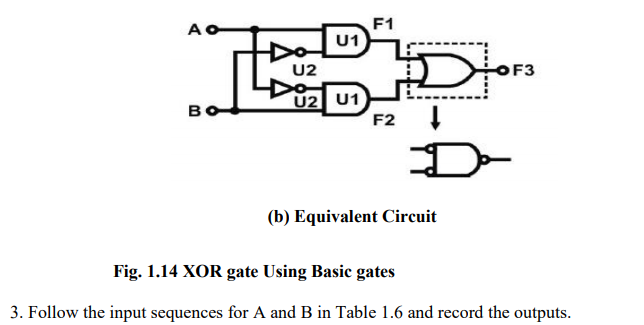
Yes it does

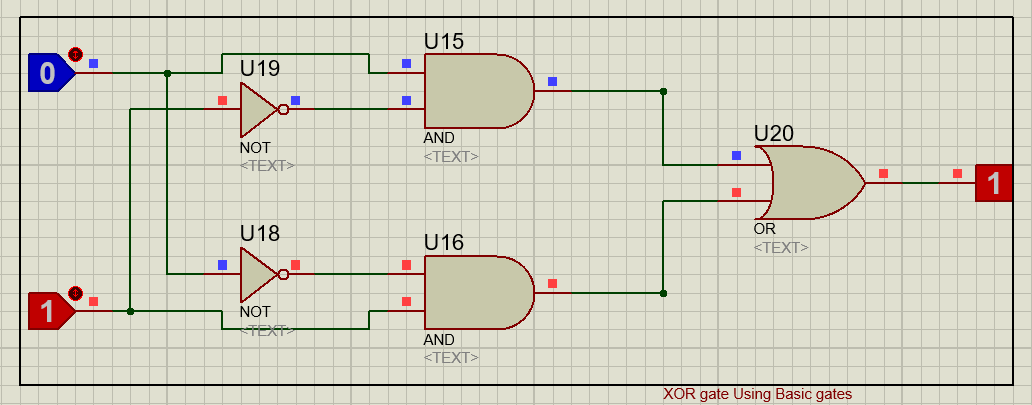
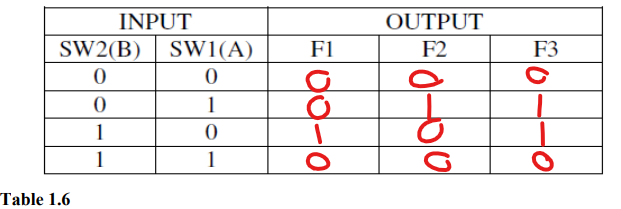


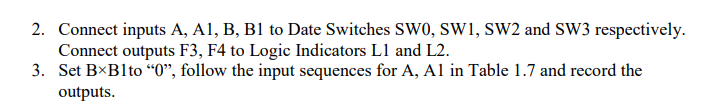
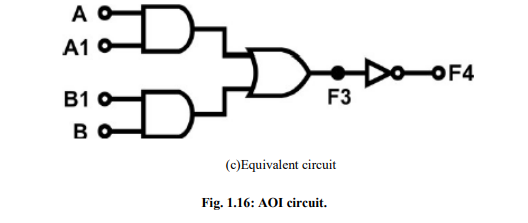
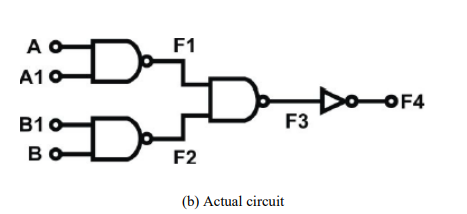


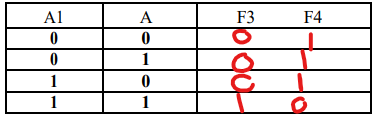










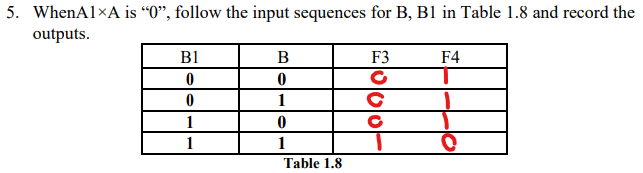


Does F3 act as an AND gate between A and A1?

Yes it does

4. WhenB×B1 is “0”, does F3 act as an AND gate between A and A1? ( F3=A×A1)

Yes it does



Does F3 act as an AND gate between B and B1?

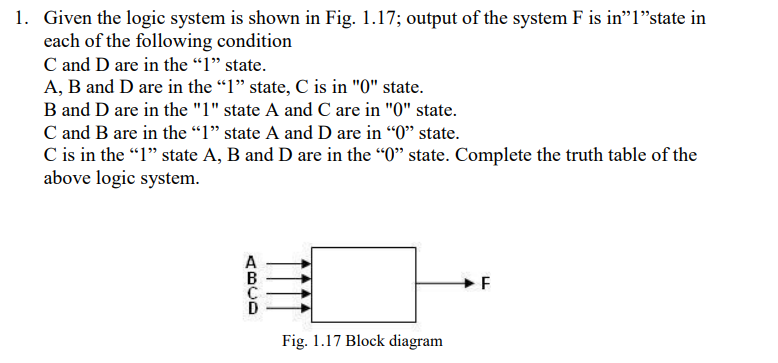
Yes

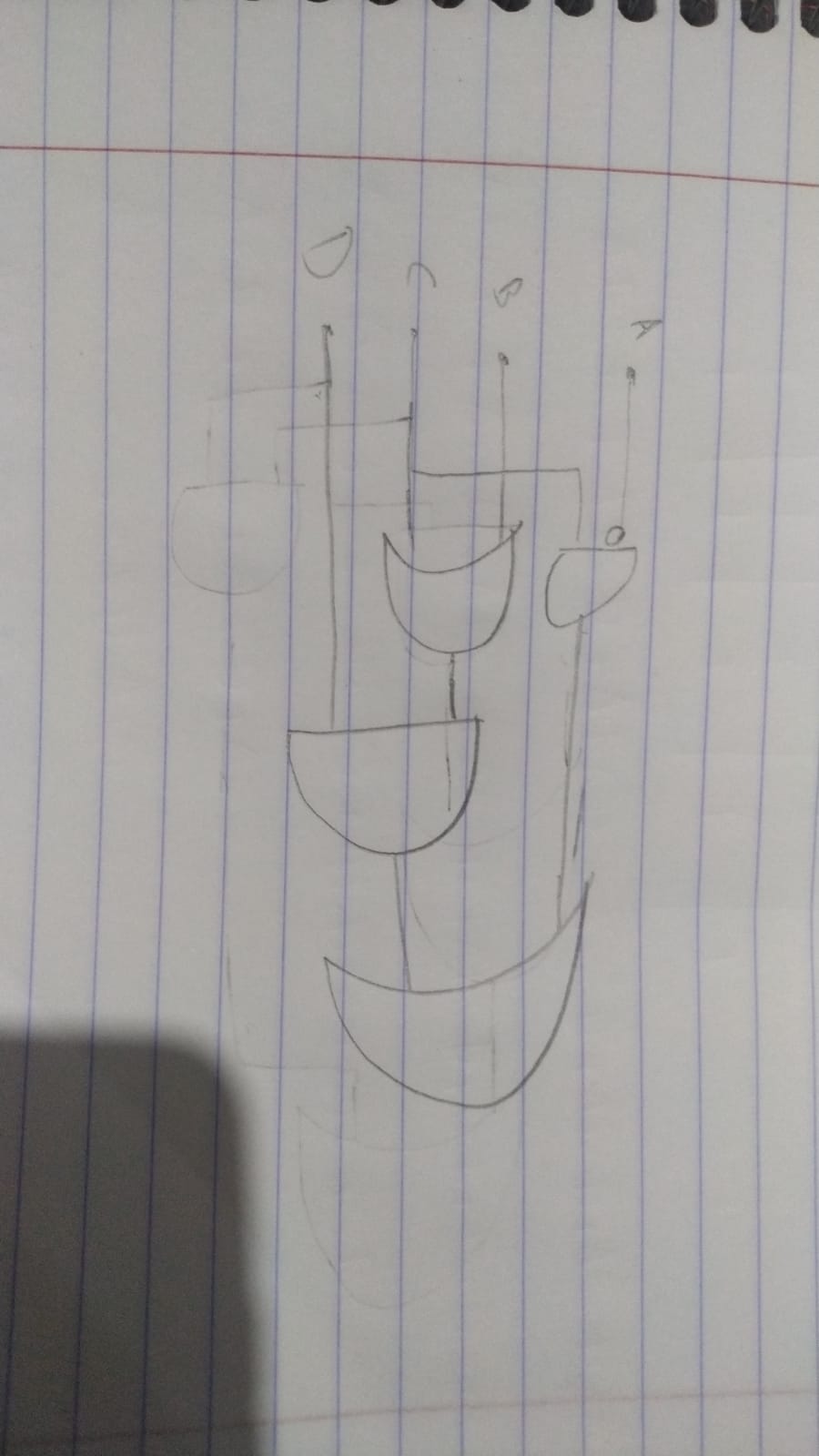
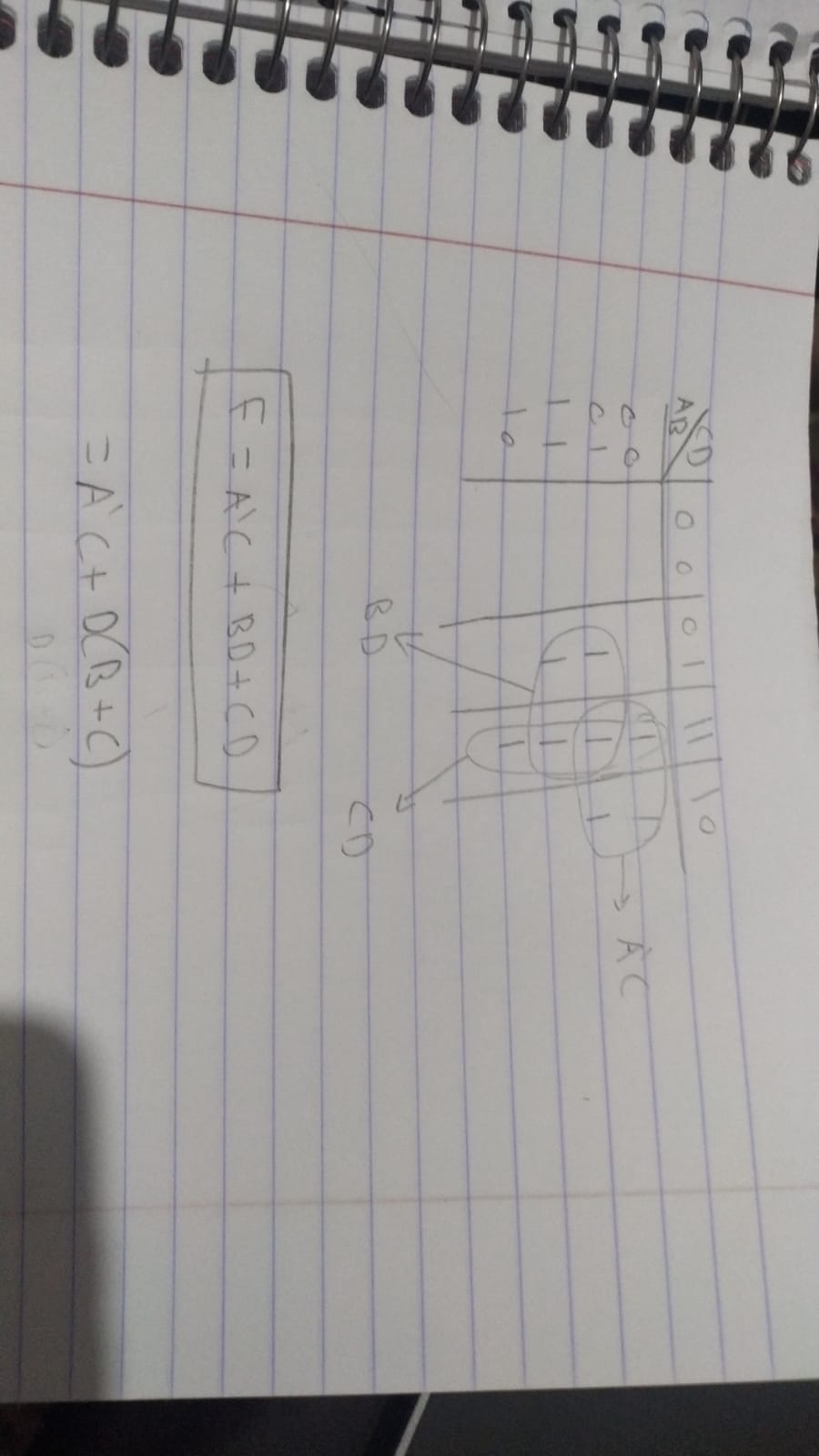
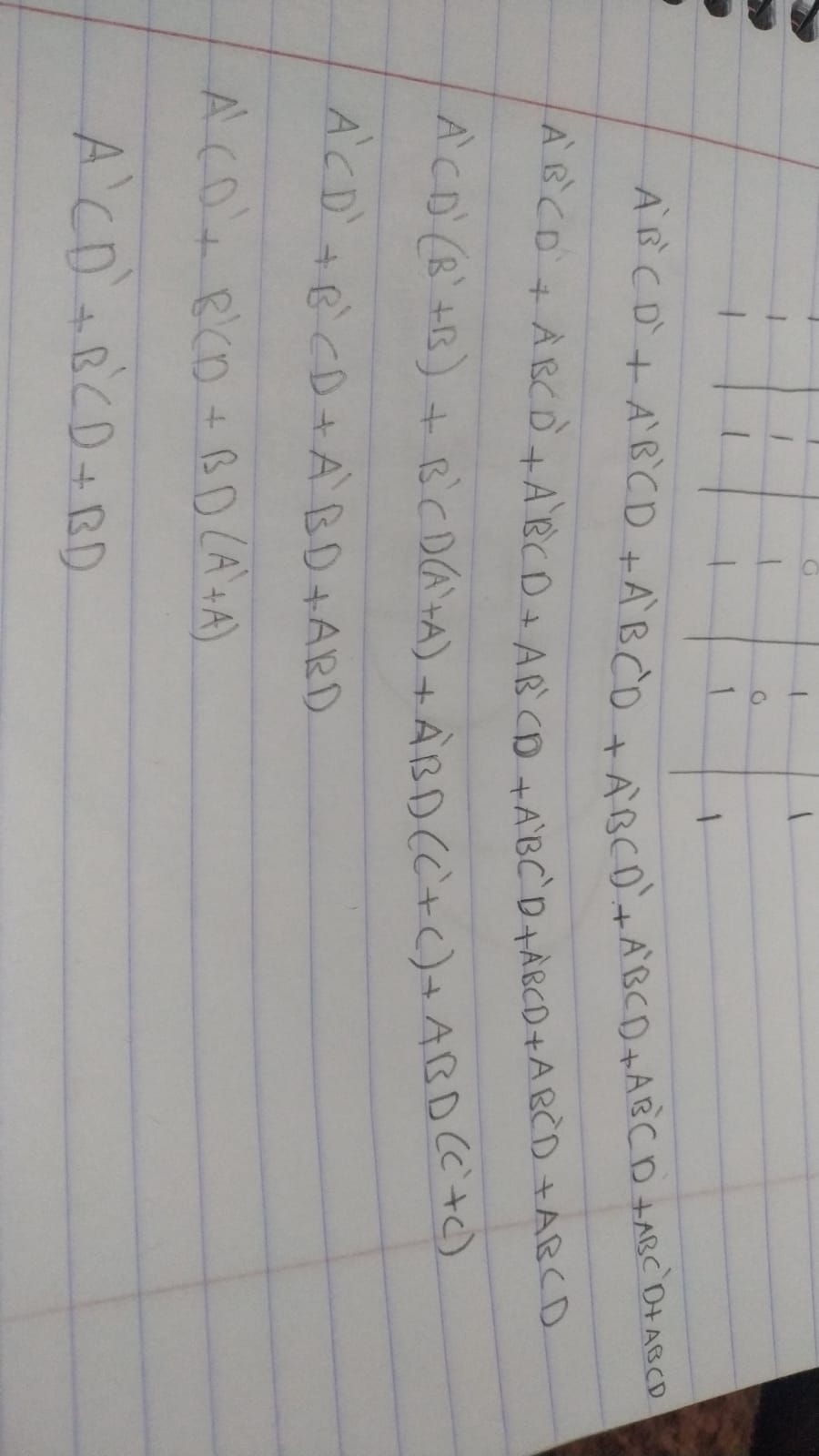
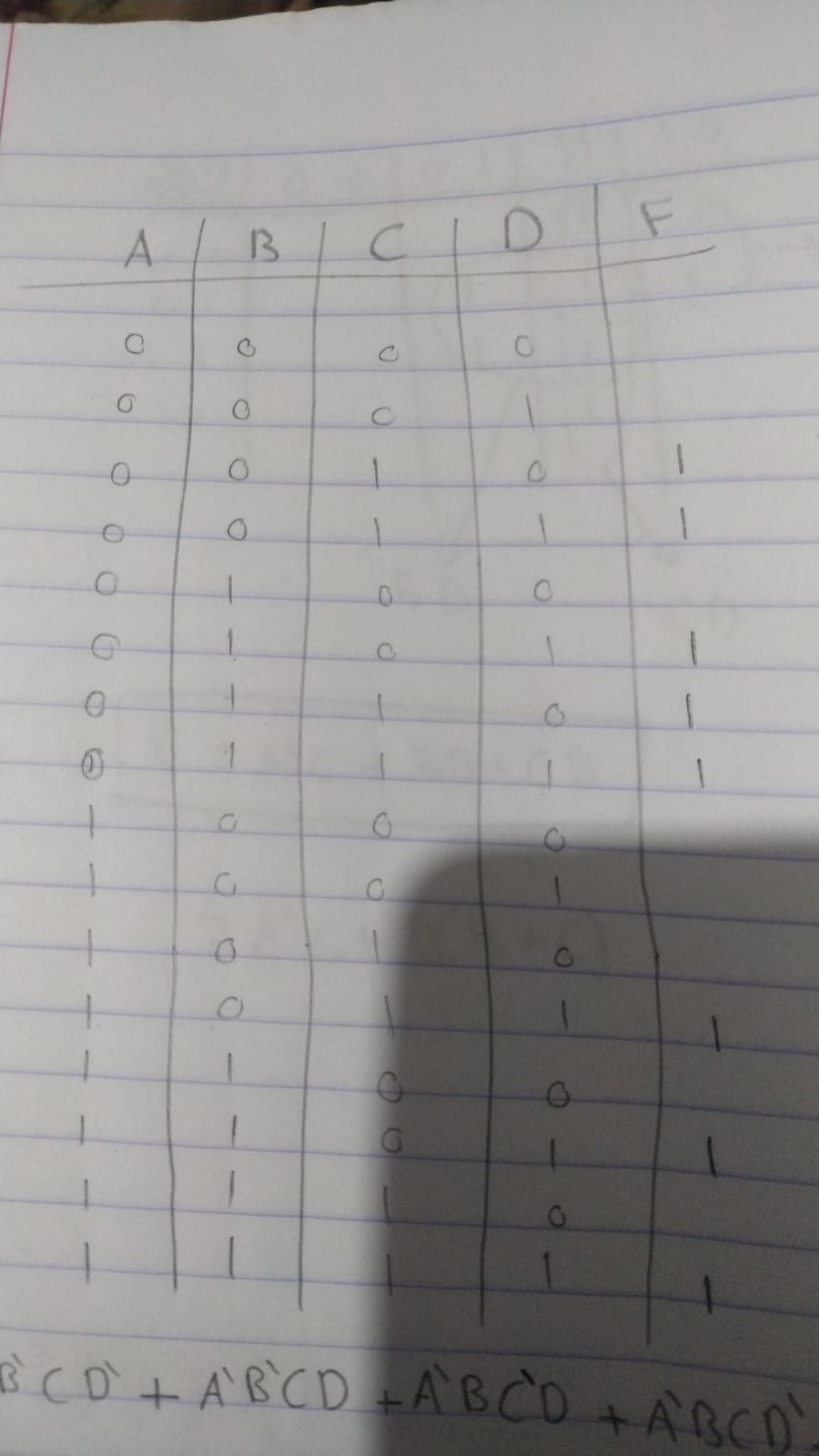
6. When A×A1 is “0”, does F3 act as an AND gate between B and B1?

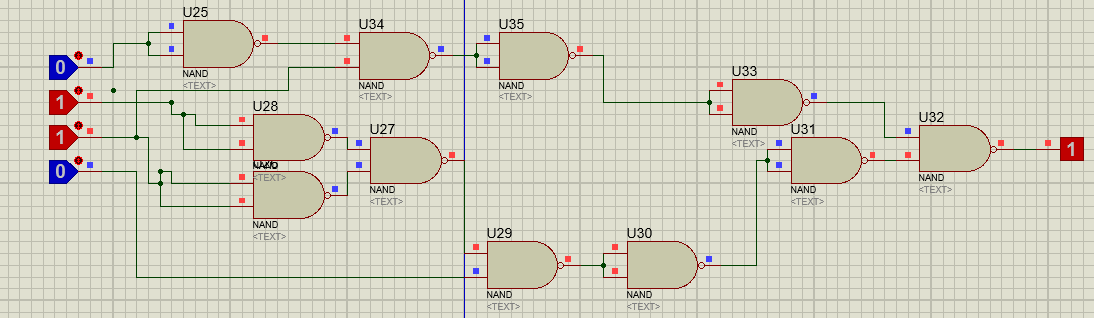
yes

Does F3 equal toA×A1+B×B1?

Yes

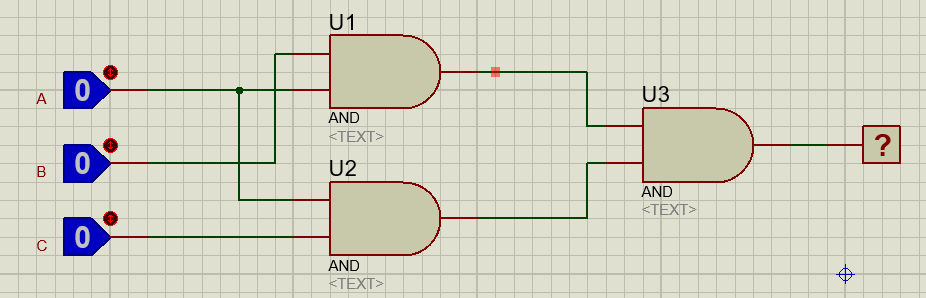






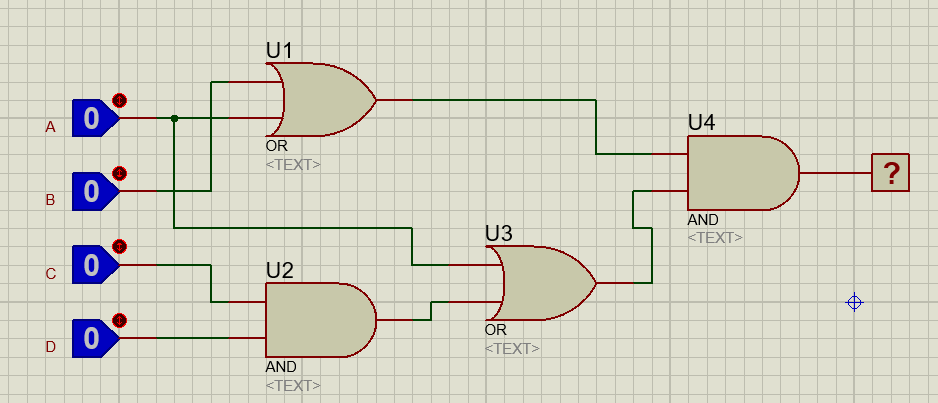
1.6 Post-lab:

1. Draw the logic diagram showing the implementation of the following Boolean equation using “AND” gates F = AB (CA).

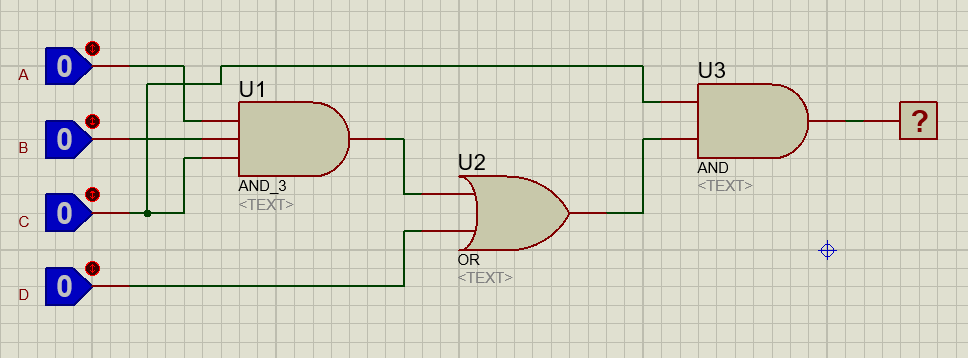


2. Draw the logic diagram of the following Boolean equations

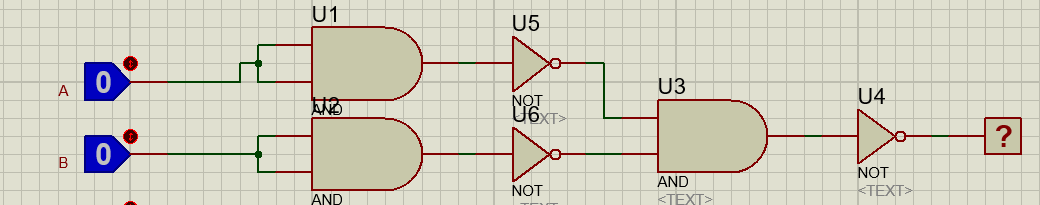
a. F2= (A+B) (CD+A)

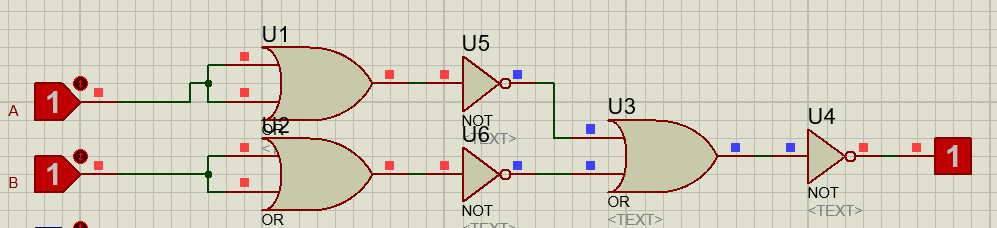


b. F3= (ABC+D) C

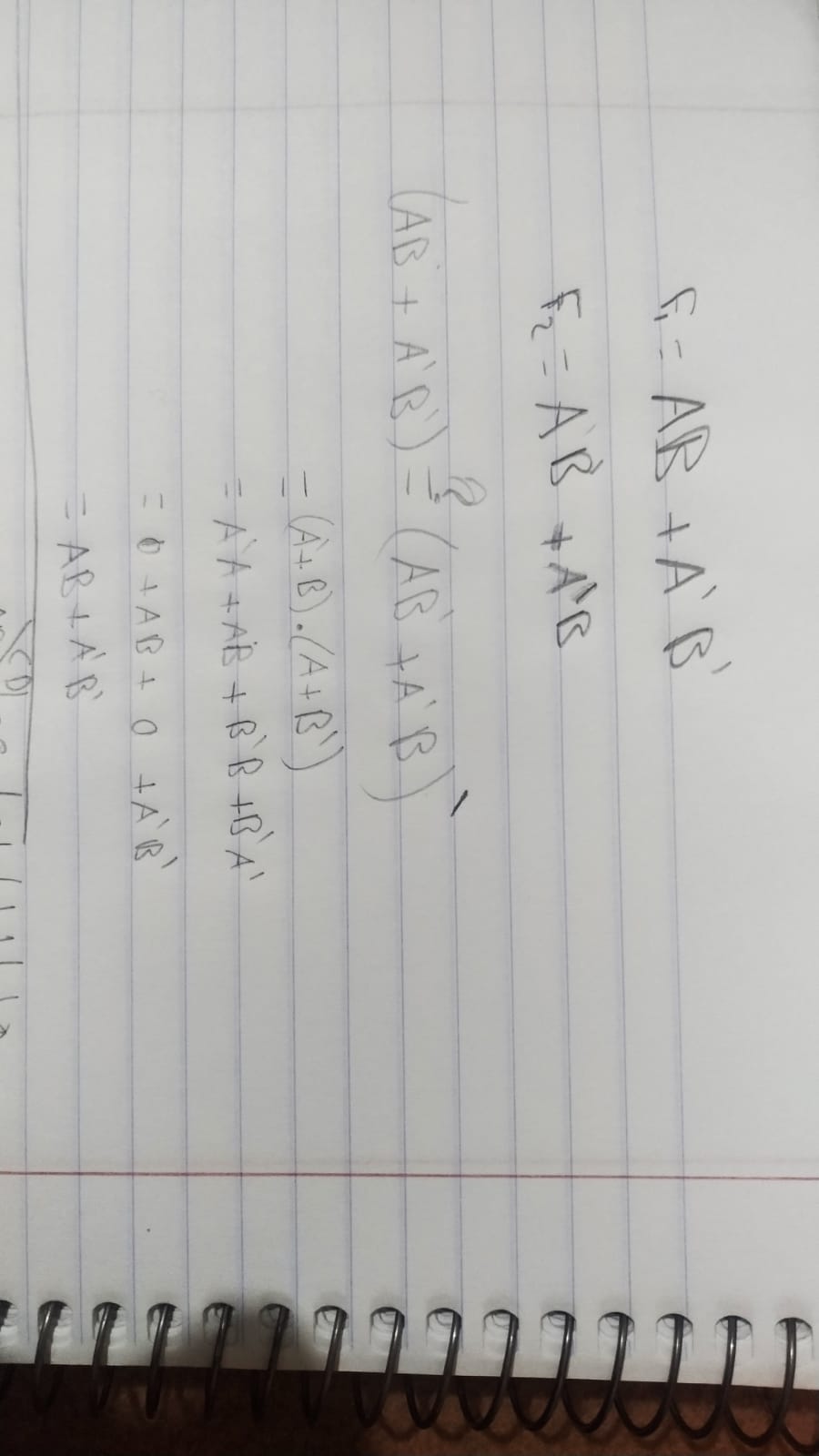


3. Implement the OR operation using AND, NOT gate.

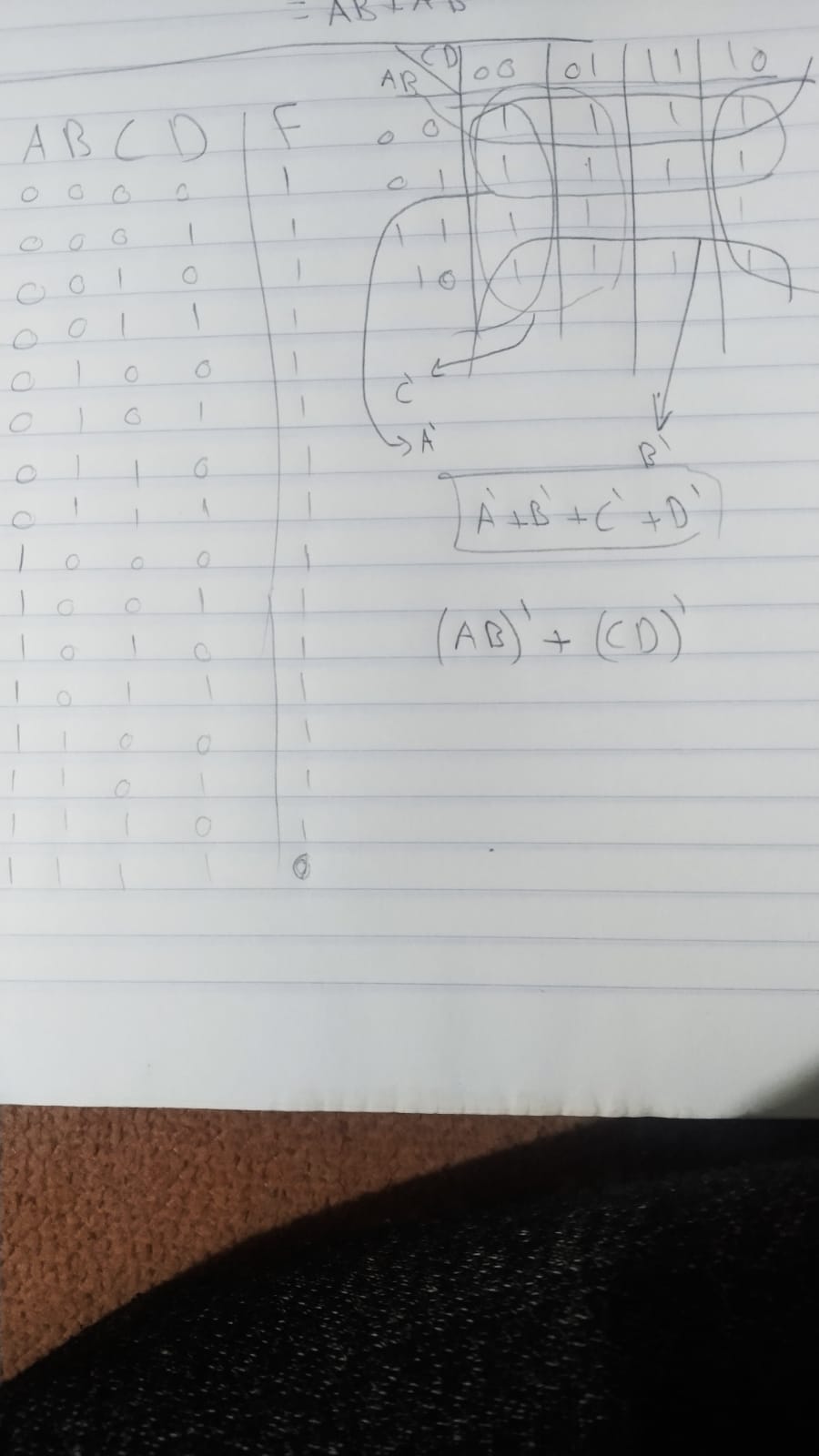
4. Implement the AND gate using OR, NOT gate. Draw the logic diagram used in both cases and write Boolean equation.

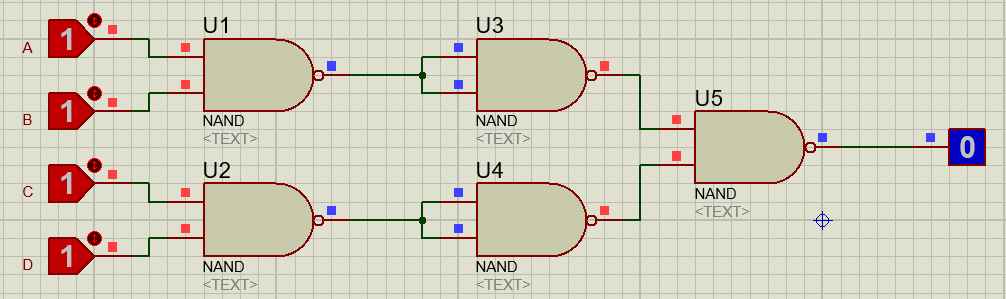


5. Prove that the equality operation Fl =AB+A’B’ is the inverse of exclusive OR operation F2=AB’+A’B (use Demorgarn’s theorem).



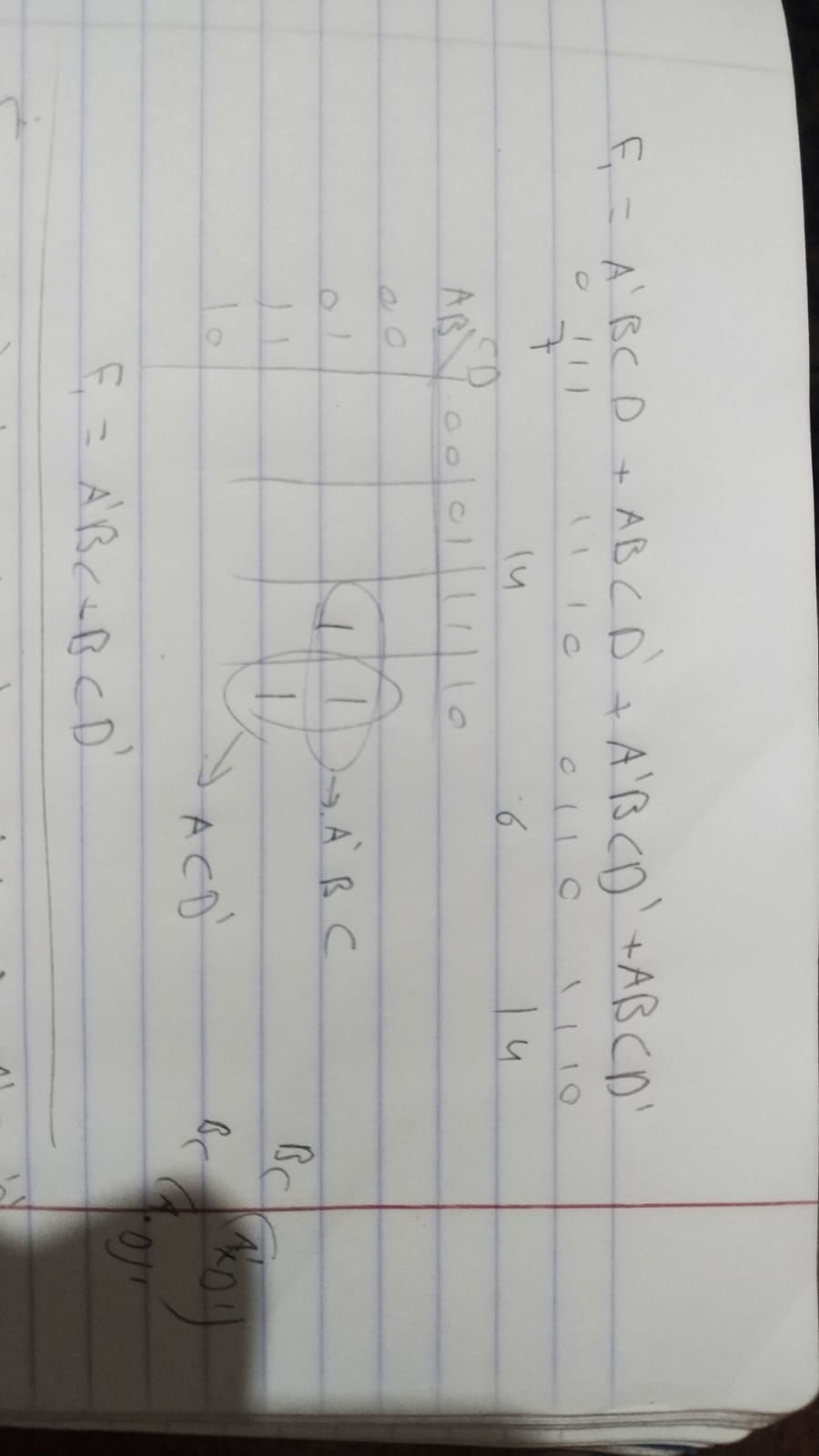
6. Suggest a logic diagram which will give a NAND gate with four inputs using two input NAND gates, Implement suggested network.

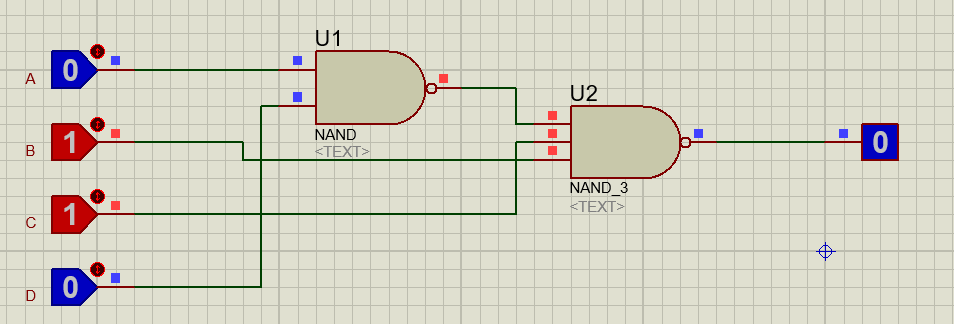




7. Show how is it possible to reduce Boolean expressions by means of karnaugh map

F1 = A'BCD + ABCD' + A'BCD' + ABCD'





F2 = A'B'C'D' + AB'CD' + A'B'CD' + A'BC'D'

Implement the minimal expressions using NAND gates.

