BIRZEIT UNIVERSITY

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

Dr. Anjad Badran

Experiment No. 5 - Comparators, Adders and Subtractors

Section 11

Islam Jihad Joma 1191375

T. Enas Jawabrah

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Abstract

In this experiment we have to learn how to use latches & flip flops, and build different kinds of them (T, JK, D, RS, SR), we have to design different circuits using them such as counters, and we have to simulate them and fill the truth tables and other tables.

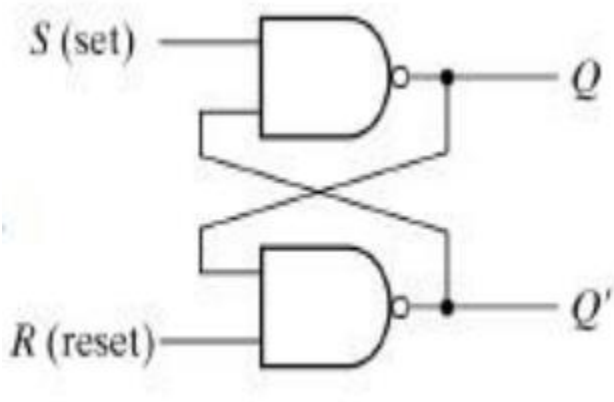
Table of content:

Introduction (Theory)

We'll make some circuits to make some functions using latches & flip flops, using different kinds of them (T, JK, D, RS, SR), We need to create one at least for each one. We'll fill the truth tables and other tables. We need to simulate them and save the data; we'll solve some tasks too.

Procedure (Discussion & Results)

SR latch

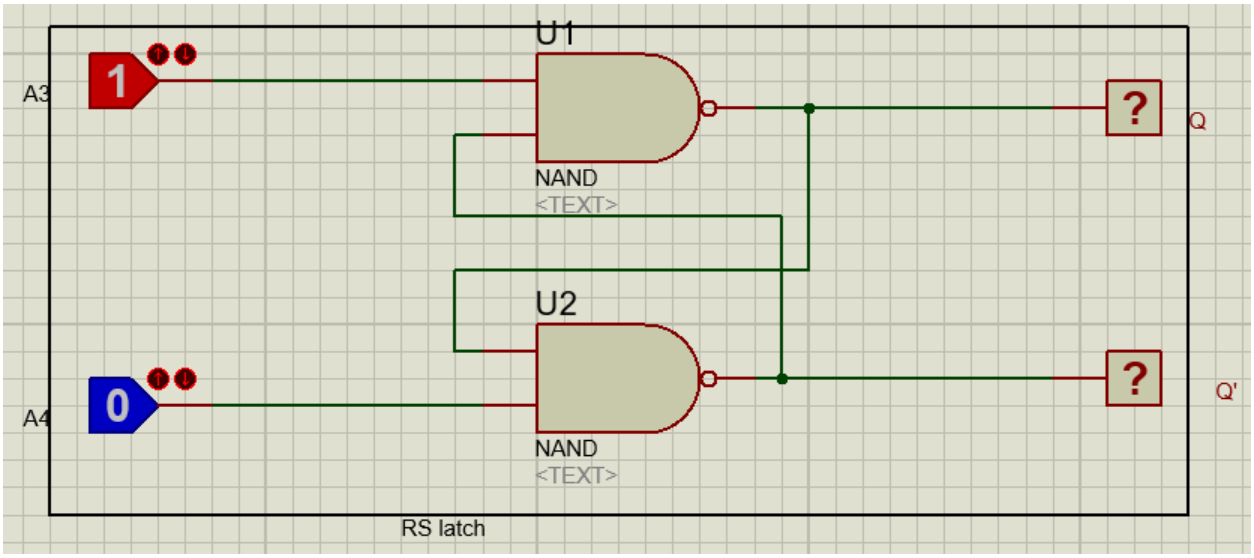


This is the results for this latch on paper

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

We used Portus of course to create the circuit, we needed the input and output buttons and the NAND gates and that's it!

I'll share a picture of the circuit



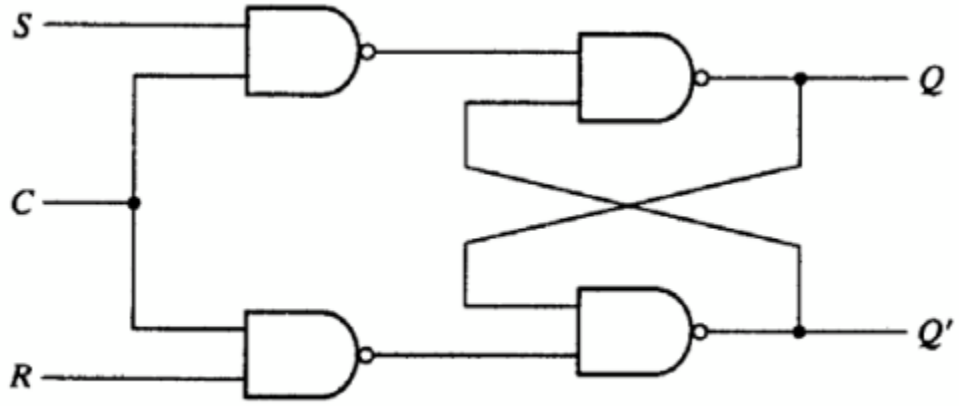
Then I simulated it and got a true result exactly like this:

A3	A4	F6	F7
0	0	1	1
0	1	1	0
1	0	0	1
1	1		

Table 5.1

and the 1 1 was the similar to the previous one before

RS latch

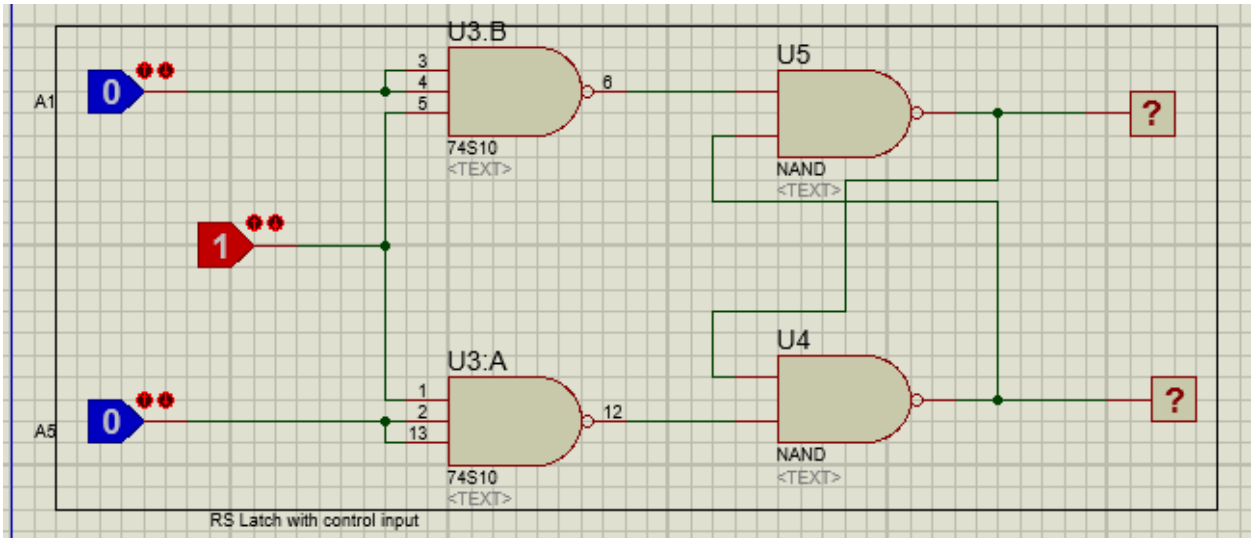


We used Portus of course to create the circuit, we needed the input and output buttons and the NAND gates.

This is the results for this latch on paper

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

I'll share a picture of the circuit



Then I simulated it and got true results exactly like this:

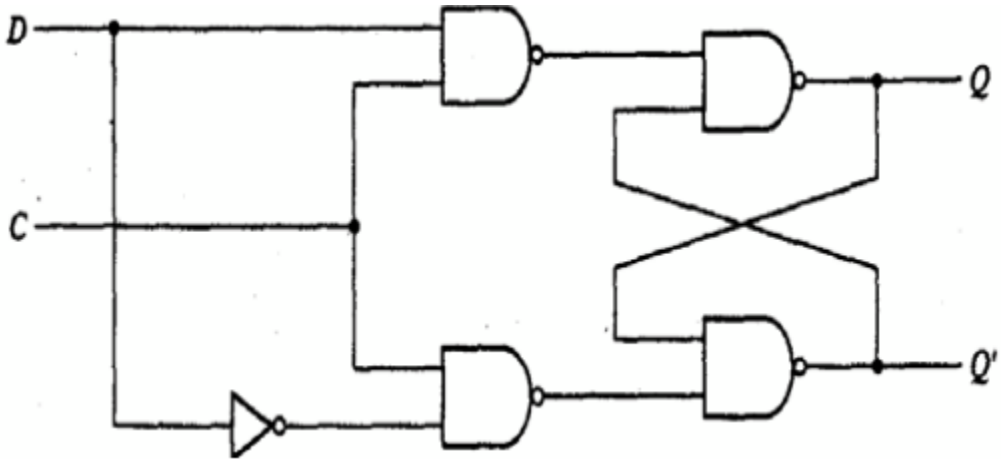
A1	A5	F6	F7
0	0		
0	1		
1	0		
1	1		

Table 5.2

when the inputs are 1 1 the output are undtermined and when the input is 0 0 the output don't change from the past change

true for all results

D-Latch

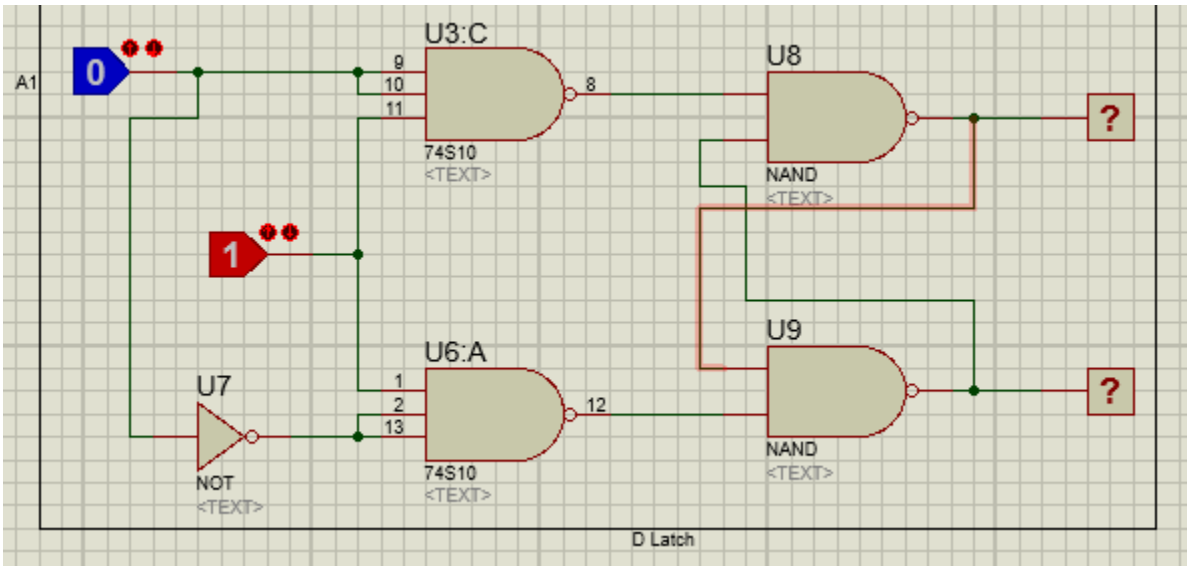


We used Portus of course to create the circuit, we needed the input and output buttons and the NAND gates.

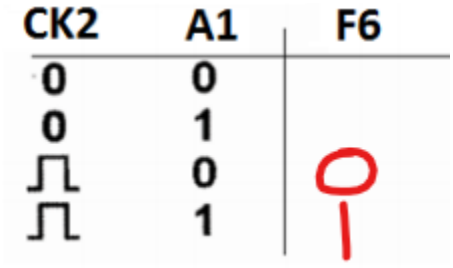
This is the results for this latch on paper

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

I'll share a picture of the circuit



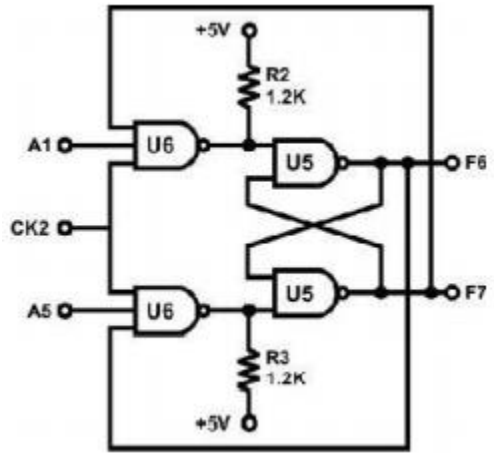
Then I simulated it and got true results exactly like this:



when the clock is 0 no change will happen for the output from the previous one

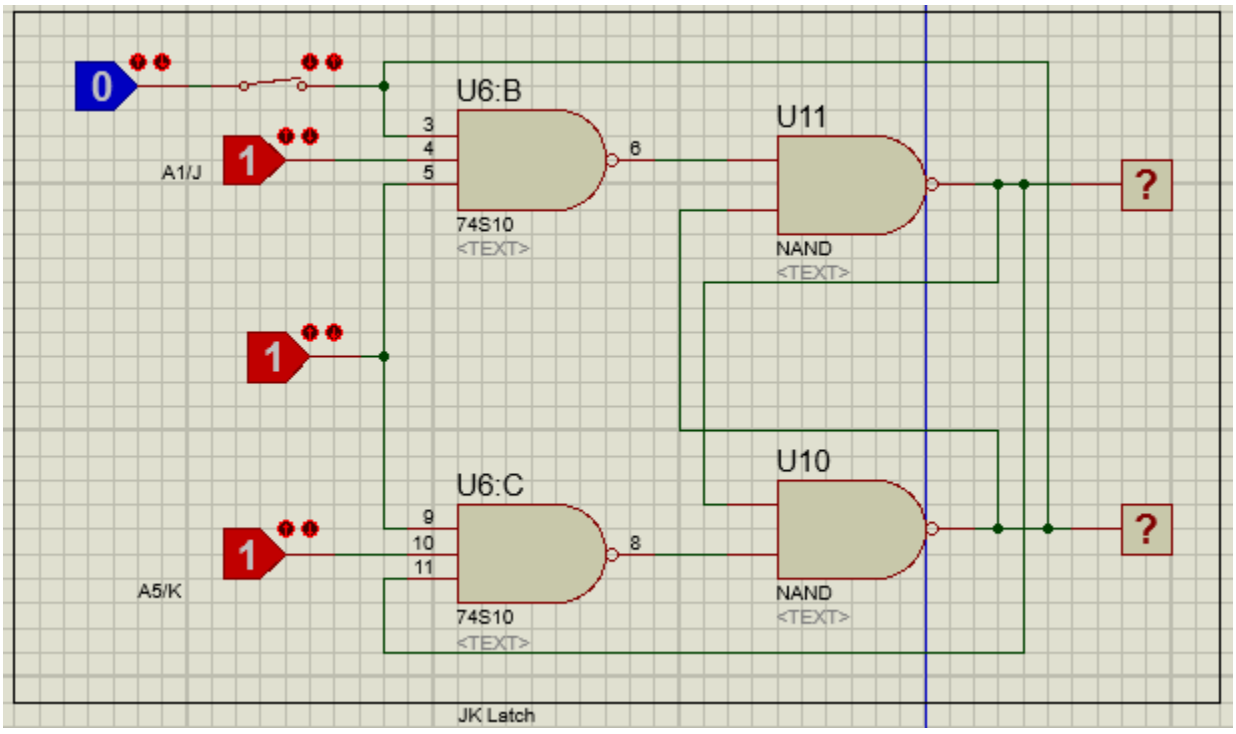
and all the results were true

JK Latch

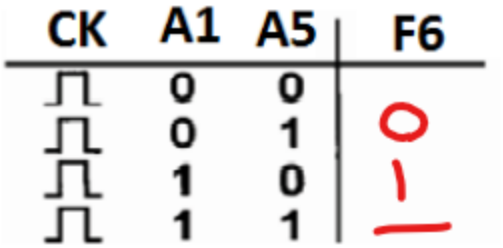


We used Portus of course to create the circuit, we needed the input and output buttons and the NAND gates.

I'll share a picture of the circuit

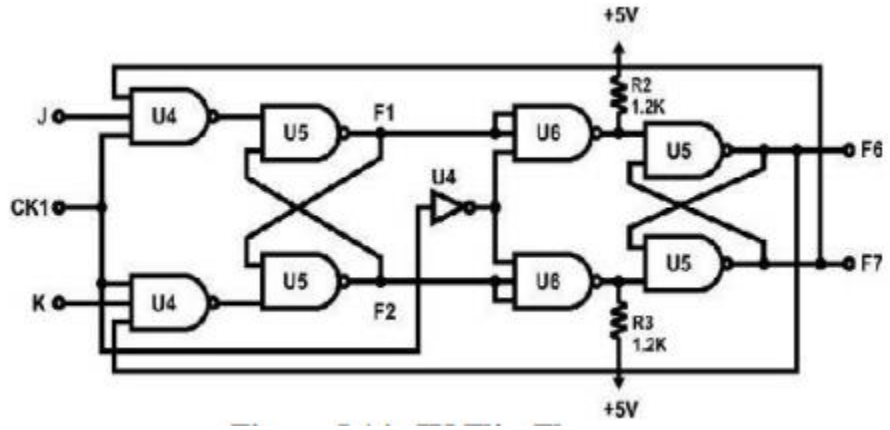


Then I simulated it and got true results exactly like this:



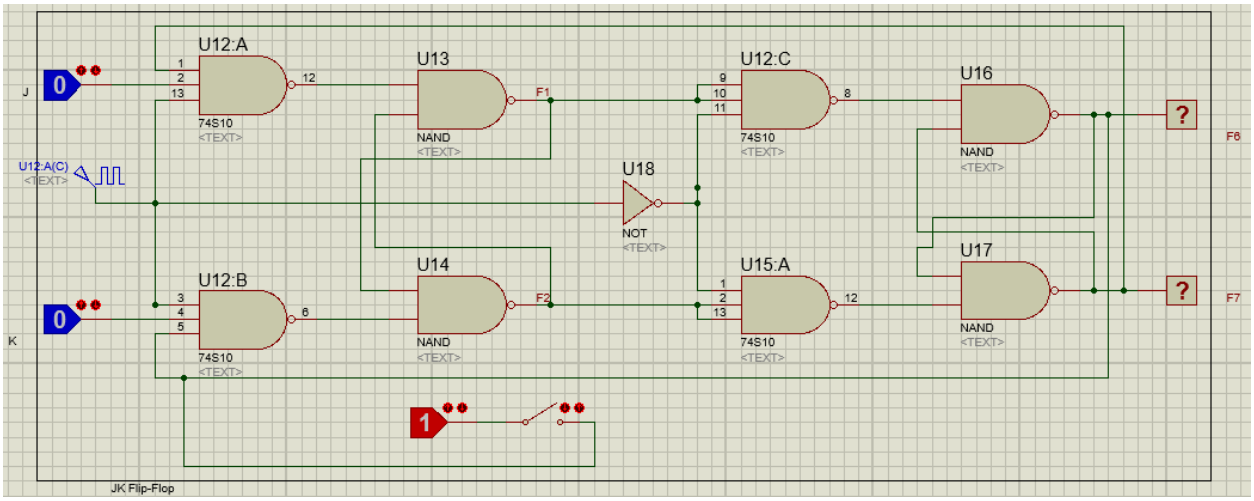
when the input is 1 1 the output toggles and when it's 0 0 no change happens

JK Flip-Flop



We used Portus of course to create the circuit, we needed the input and output buttons and the NAND gates and NOT gate.

I'll share a picture of the circuit

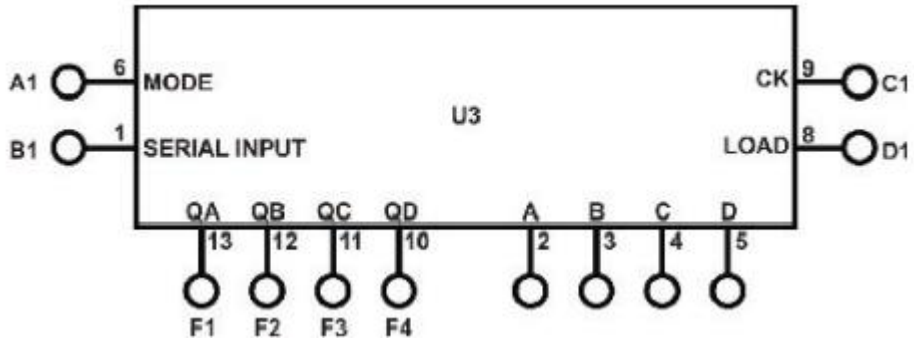


Then I simulated it and got true results exactly like this:

CK	K	J	F1	F2	F6	F7
⎍	0	0				
⎍	0	1	0	1	0	1
⎍	1	0	1	0	1	0
⎍	1	1	1	0	1	0
⎍	1	1	0	1	0	1

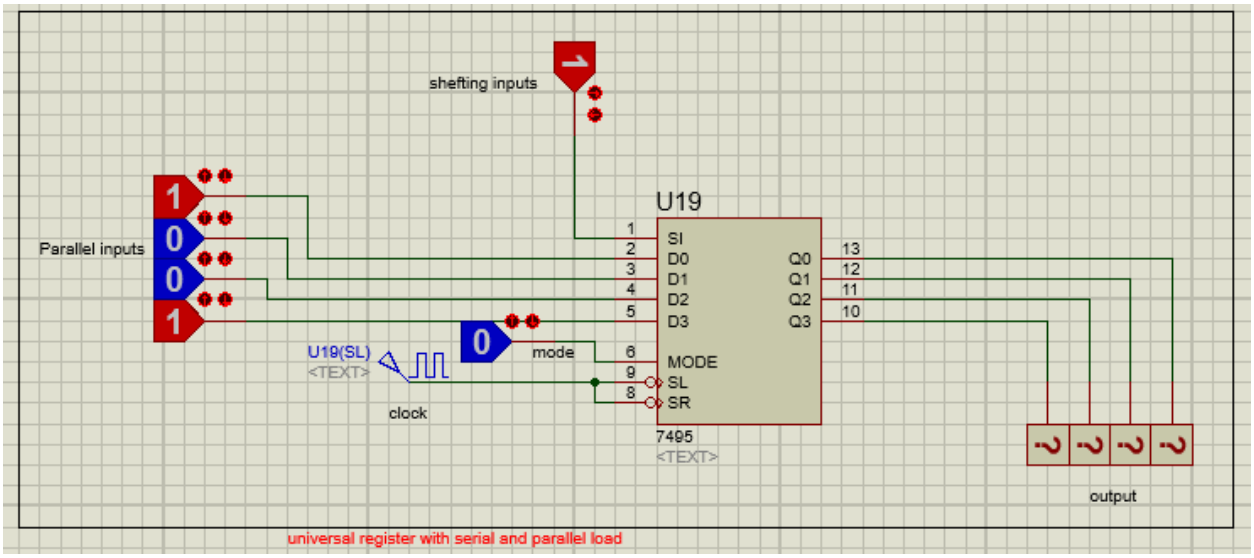
when it's 0 0 the output doesn't change, all of the results are true

universal register with serial and parallel load



We used Portus of course to create the circuit, we needed the input and output buttons and this IC.

I'll share a picture of the circuit



Then I simulated it and got true results exactly like this:

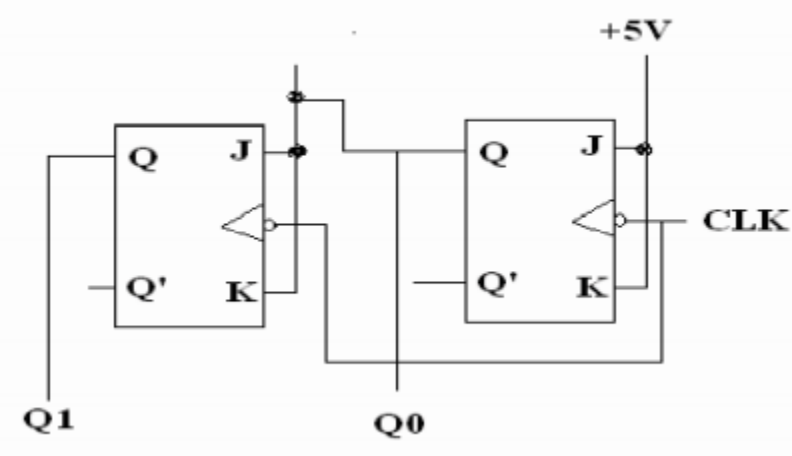
Input		Output			
A1	C1	L3	L2	L1	L0
0					
0					
0					
1					

I used 1 for all inputs and the results were true

Input					Output			
D1	D	C	B	A	L3	L2	L1	L0
	0	0	1	0				
	1	0	1	0				
	1	1	1	0				
	0	1	1	1				
	0	1	1	0				

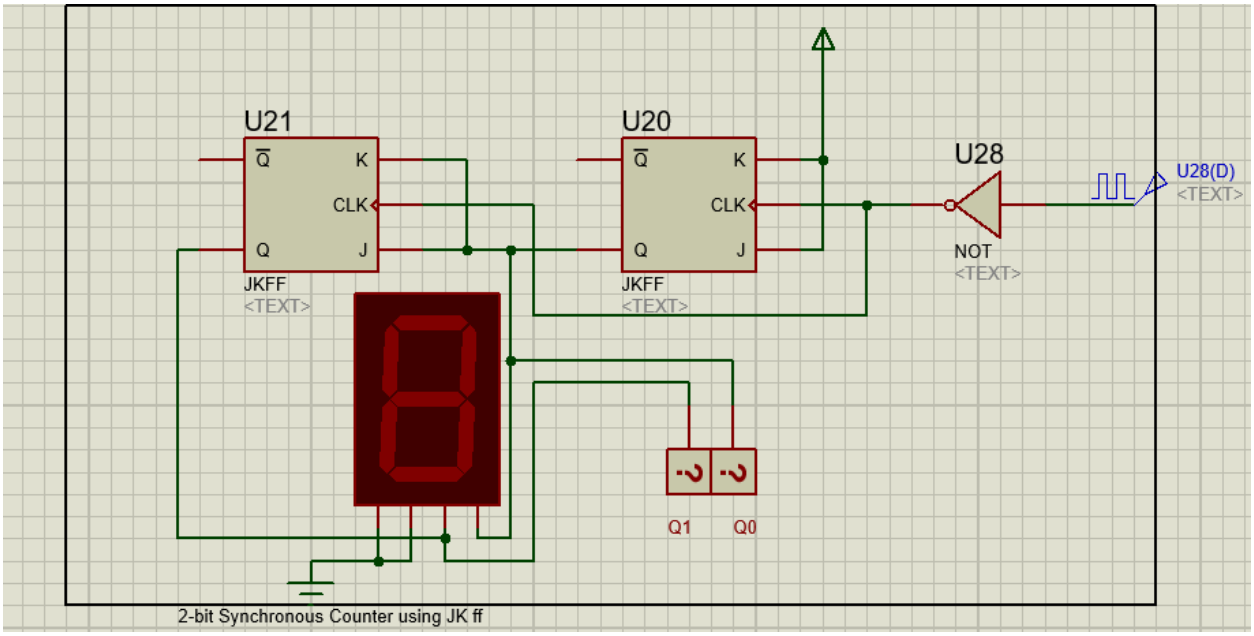
Table 5.8

2-bit Synchronous Counter

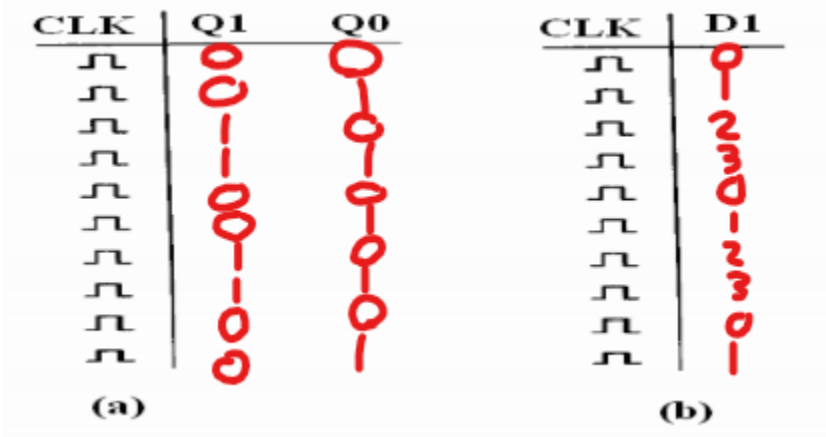


We used Portus of course to create the circuit, we needed the input and output buttons and 2 JK flip flops.

I'll share a picture of the circuit

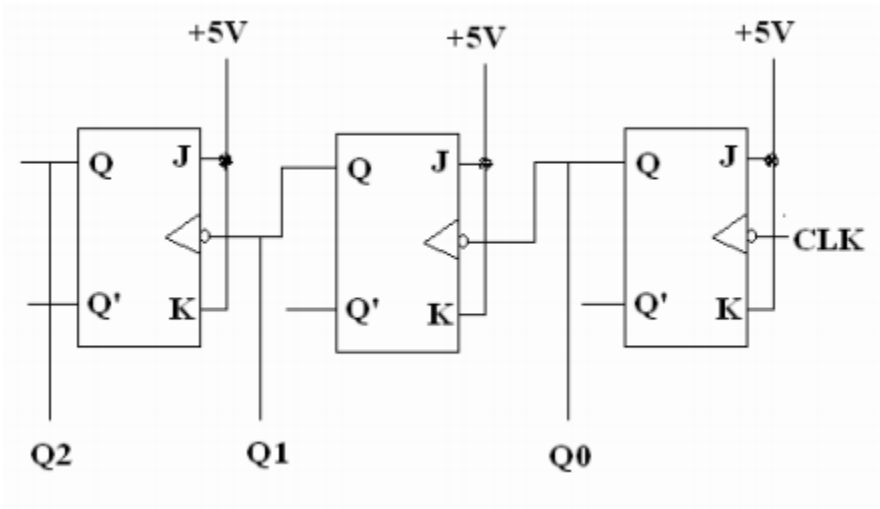


Then I simulated it and got true results exactly like this:



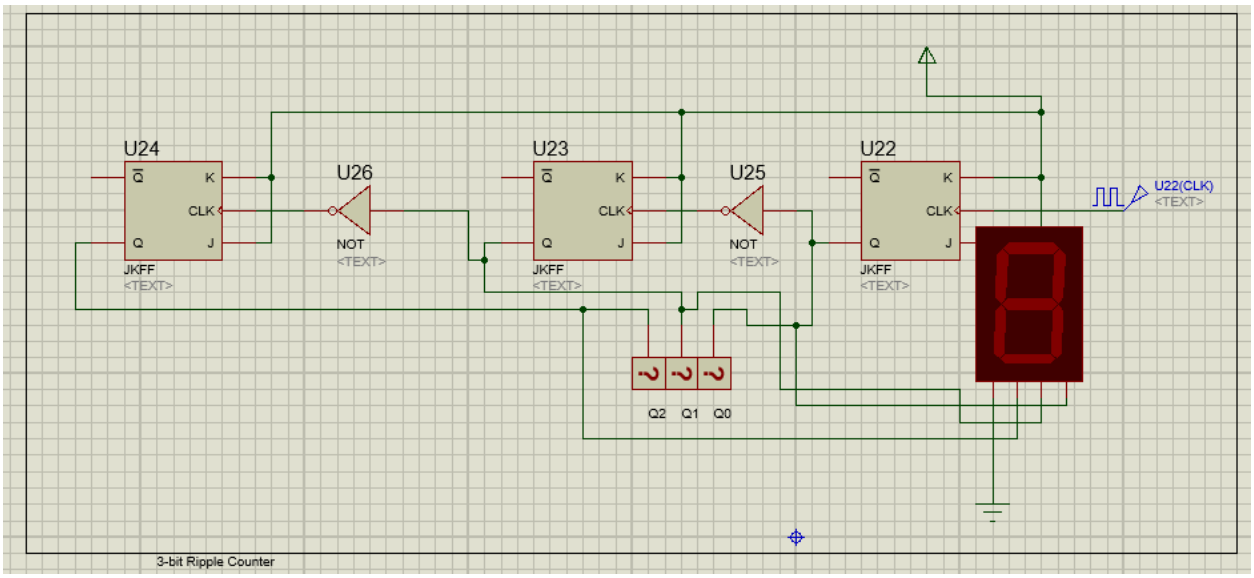
as a counter the results are true

3-bit (divide-by-eight) Ripple Counter

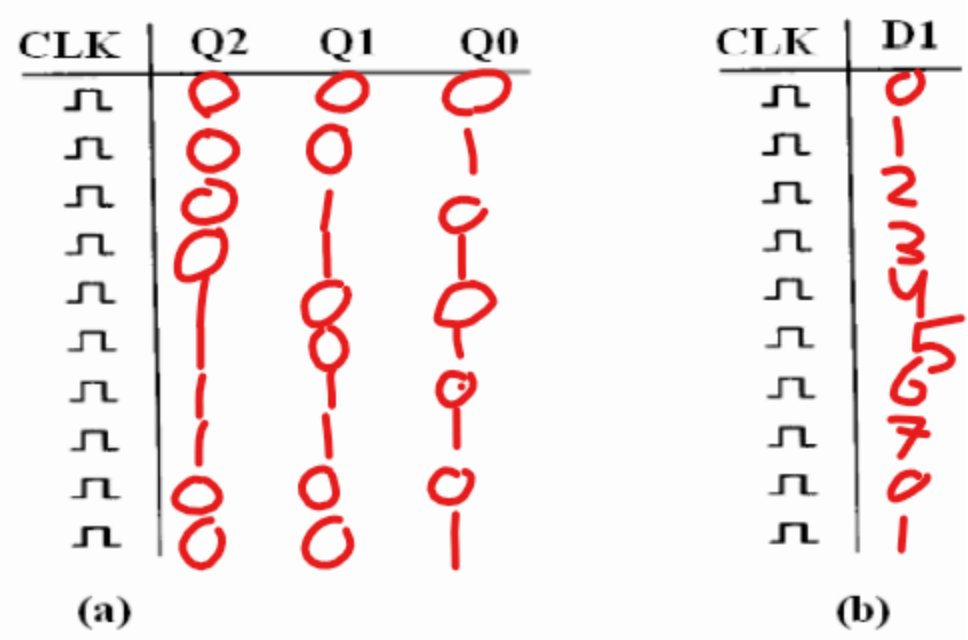


We used Portus of course to create the circuit, we needed the input and output buttons and 3 JK flip flops.

I'll share a picture of the circuit

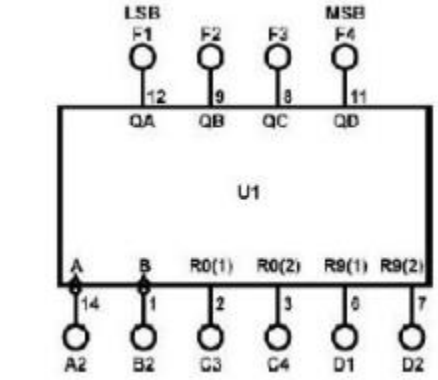


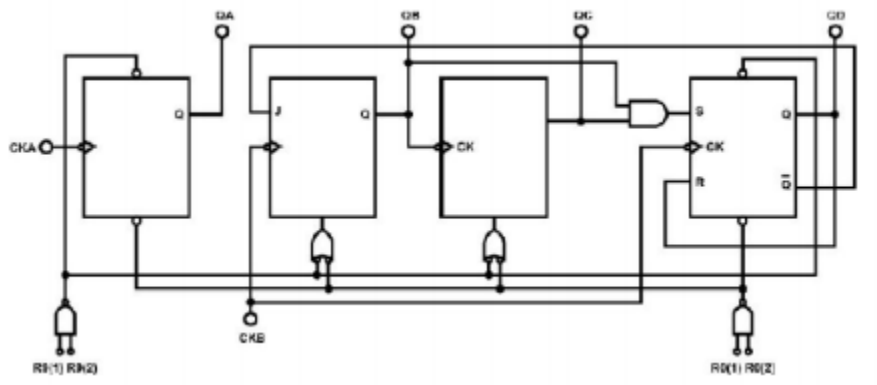
Then I simulated it and got true results exactly like this:



as a counter the results are true

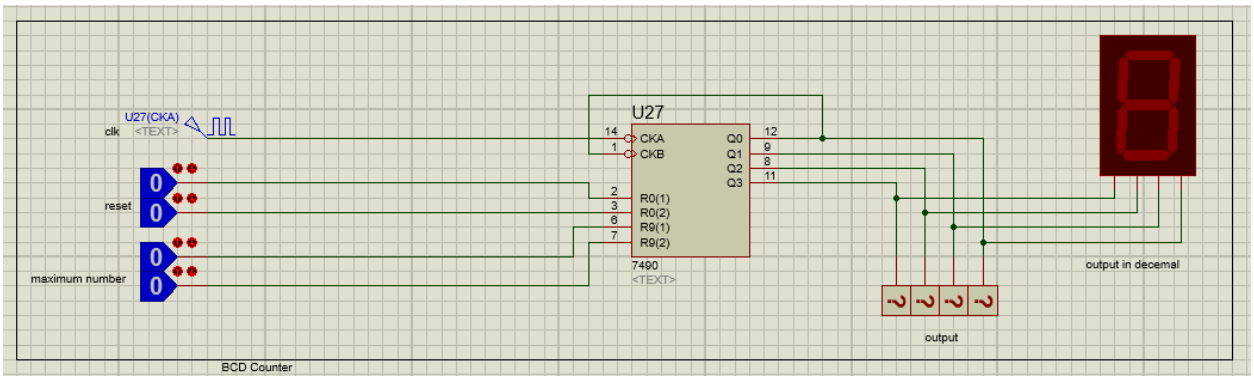
BCD Counter





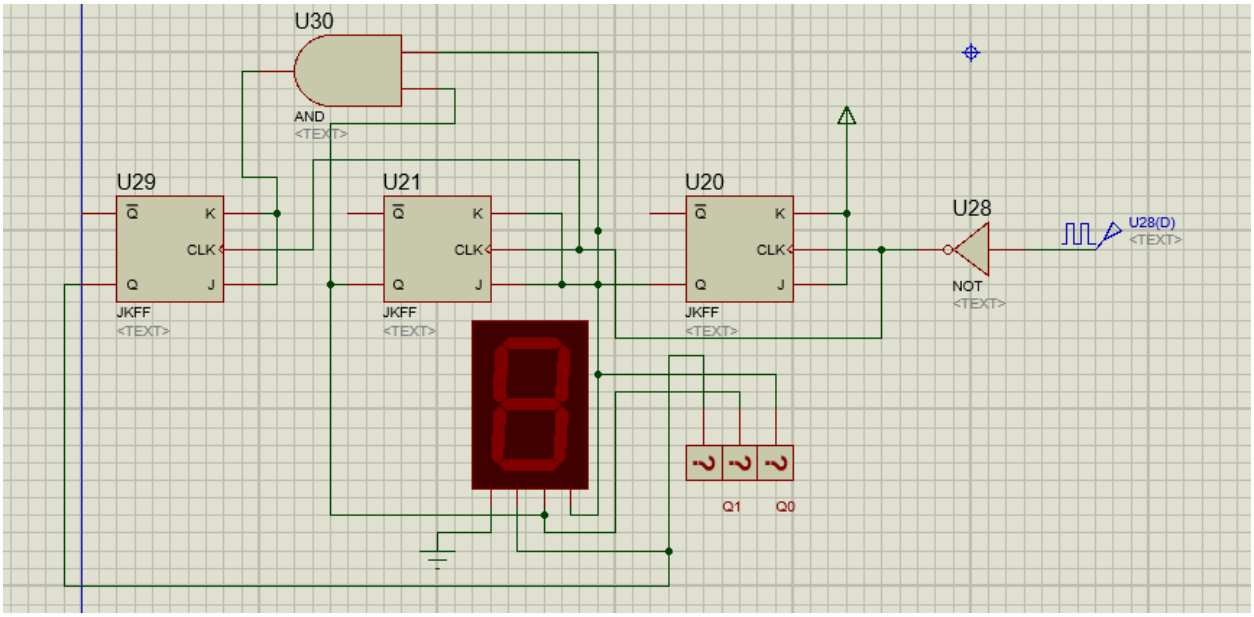
We used Portus of course to create the circuit, we needed the input and output buttons and BCD IC.

I'll share a picture of the circuit



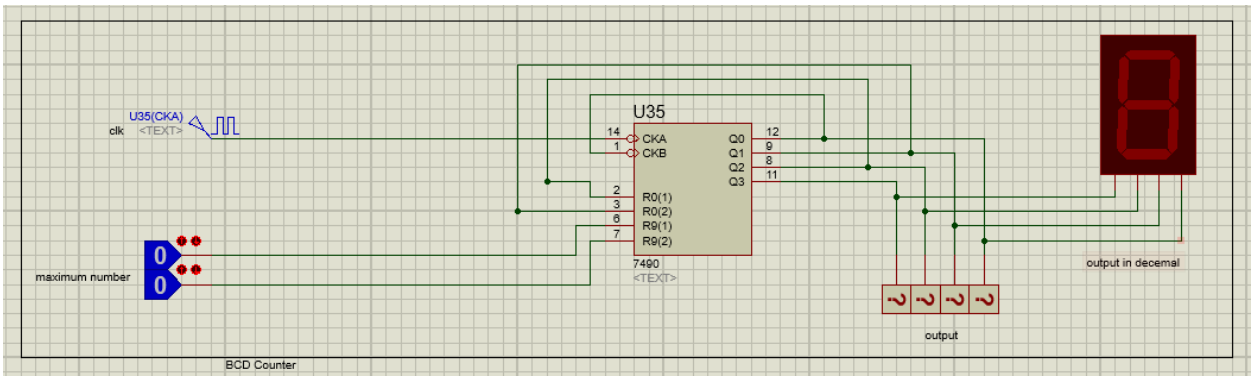
This circuit didn't ask for table but in general it count from 0 to 9 and start again from zero

Task2: Modify the circuit in Figure 5.16 to be 3-bitSynchronous Counter. Attach the design with this experiment report.

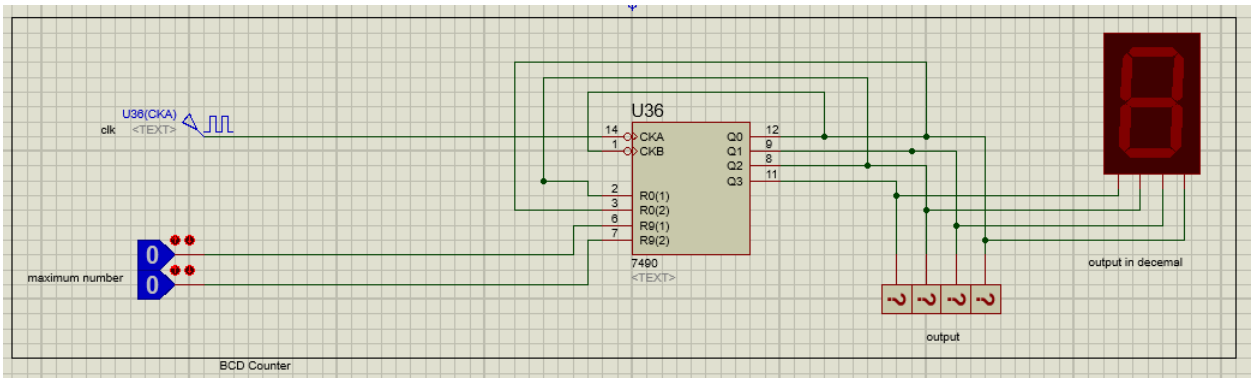


Task3: change the connection of counter in Figure.19 to count from:

- 0-to-5



- 0-to4



DISCUSSION

Answer the following questions:

1. Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?
   Because latches are level sensitive and Flipflops are edge sensitive
   Latches are less accurate than flip flops
2. What is the disadvantage of the RS flip flop?
   we cannot have input 1,1

3. What is the difference between “synchronous” and “ripple” counters?
   Ripple Counter: different flip flops are triggered with different clock, not simultaneously.
   Synchronous Counter: all flip flops are triggered with same clock simultaneously

Conclusion

In this experiment I became familiar flip flops and latches and build counters and some circuits and how to connect them together. And I have verified the correctness of my work by using the simulation button for every circuit and compared it with the tables in the PDF file we got from the teacher. Now I can create more and more counters and circuits using flip flops and latches.

References

In this experiment I didn’t get help from outside the ALL Experiments PDF, only my own work.

Appendix

I didn’t get help from outside the ALL Experiments PDF, only my own work.