Experiment 9

Arithmetic Elements

9-1 Arithmetic Logic Unit (ALU) Circuit

OBJECTIVES

1. To understand functions and applications of the ALU, or arithmetic logic unit.
2. To perform arithmetic and logic operations using the 74181 ALU IC.
3. To understand the construction and applications of parity generators.
4. To generate parity bit using XOR gates and parity generator IC.

EQUIPMENT REQUIRED

1. KL-22001 Basic Electricity Circuit Lab.
2. KL-26005 Combinational Logic Circuit Experiment Module (5).
3. KL-26002 Combinational Logic Circuit Experiment Module (2)

Prelab:

Prepare all parts of your experiment.

DISCUSSION

In this experiment the 74181 ALU IC will be used to introduce the concept of ALU. Its logic diagram is shown in Fig. 9.1.1.
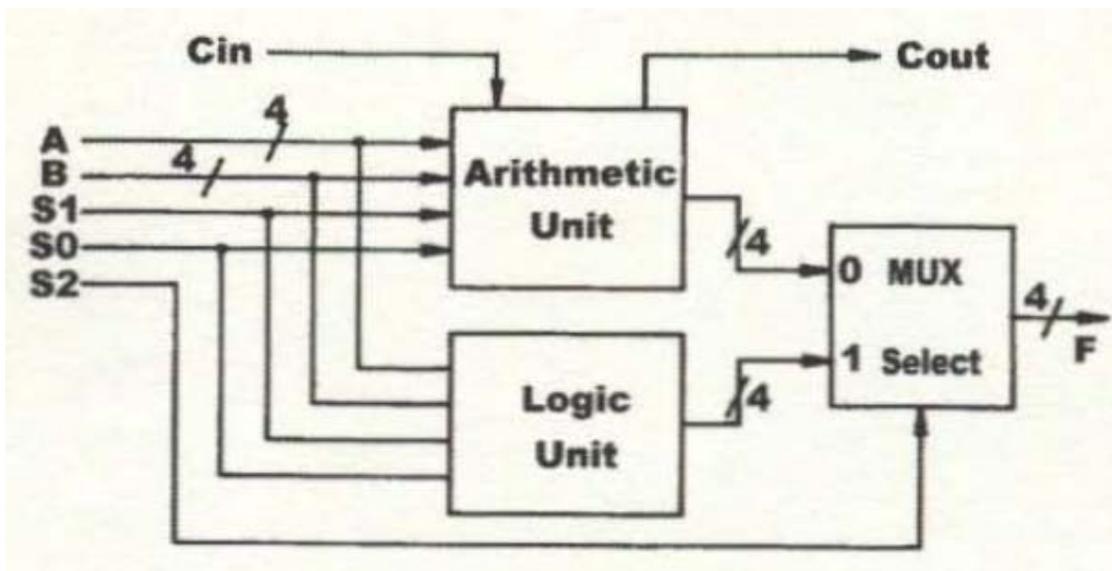
Fig. 9-1-1 ALU block diagram

It consists of two major parts: the arithmetic unit and the logic unit. The output, either arithmetic or logic, is selected by a multiplexer (MUX). S2 is the selector gate on the MUX and its state will determine the output of the ALU.

When S2=0, arithmetic operation is executed.
When S2=1, logic operation is executed.

Fig. 9-1-2 shows the pin assignment and Table 9-1-1 is the function table for the 74181.
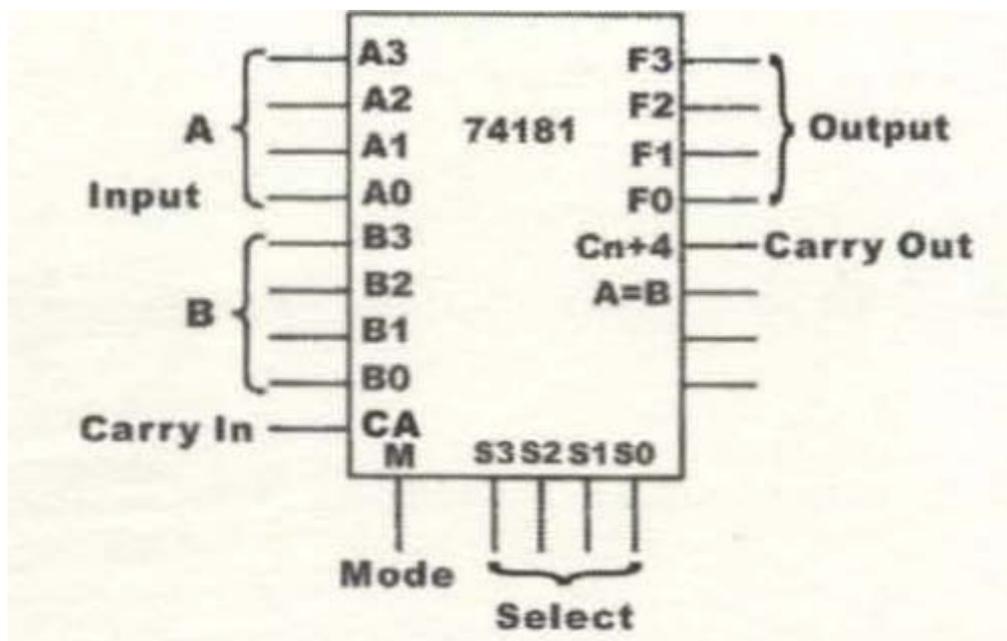

Fig. 9-1-2 74181 pin assignment

| SELECTION | | | | ACTIVE LOW DATA | | | ACTIVE LOW DATA | | |
S3	S2	S1	S0	M=H LOGIC FUNCTIONS	M=L ARITHMETIC OPERATIONS Cn=L (no carry)	Cn=H (with carry)	M=H LOGIC FUNCTIONS	M=L ARITHMETIC OPERATIONS $\overline{Cn}$=H (no carry)	$\overline{Cn}$=L (with carry)
L	L	L	L	$F=\overline{A}$	$F=A$ MINUS 1	$F=A$	$F=\overline{A}$	$F=A$	$F=A$ PLUS 1
L	L	L	H	$F=\overline{AB}$	$F=AB$ MINUS 1	$F=AB$	$F=\overline{A}+B$	$F=A+B$	$F=(A+B)$ PLUS 1
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ MINUS 1	$F=A\overline{B}$	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ PLUS 1
L	L	H	H	$F=1$	$F=$ MINUS 1 (2's, COMP)	$F=$ZERO	$F=0$	$F=$ MINUS 1 (2's COMP)	$F=$ZERO
L	H	L	L	$F=\overline{A+B}$	$F=A$ PLUS $(A+\overline{B})$	$F=A$ PLUS $(A+\overline{B})$ PLUS 1	$F=\overline{AB}$	$F=A$ PLUS $A\overline{B}$	$F=A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F=\overline{B}$	$F=AB$ PLUS $(A+\overline{B})$	$F=AB$ PLUS $(A+\overline{B})$ PLUS 1	$F=\overline{B}$	$F=(A+B)$ PLUS $A\overline{B}$	$F=(A+B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F=\overline{A\oplus B}$	$F=A$ MINUS B MINUS 1	$F=A$ MINUS B	$F=A\oplus B$	$F=A$ MINUS B MINUS 1	$F=A$ MINUS B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	$F=A+\overline{B}$ PLUS 1	$F=A\overline{B}$	$F=A\overline{B}$ MINUS	$F=A\overline{B}$
H	L	L	L	$F=\overline{A}B$	$F=A$ PLUS $(A+B)$	$F=A$ PLUS $(A+B)$ PLUS 1	$F=\overline{A}+B$	$F=A$ PLUS AB	$F=A$ PLUS AB PLUS 1
H	L	L	H	$F=A\oplus B$	$F=A$ PLUS B	$F=A$ PLUS B PLUS 1	$F=\overline{A\oplus B}$	$F=A$ PLUS B	$F=A$ PLUS B PLUS 1
H	L	H	L	$F=B$	$F=A\overline{B}$ PLUS $(A+B)$	$F=A\overline{B}$ PLUS $(A+B)$ PLUS 1	$F=B$	$F=(A+\overline{B})$ PLUS AB	$F=(A+\overline{B})$ PLUS AB PLUS 1
H	L	H	H	$F=A+B$	$F=(A+B)$	$F=(A+B)$ PLUS 1	$F=AB$	$F=AB$ MINUS 1	$F=AB$
H	H	L	L	$F=0$	$F=A$ PLUS A	$F=A$ PLUS A PLUS 1	$F=1$	$F=A$ PLUS A	$F=A$ PLUS A PLUS 1
H	H	L	H	$F=A\overline{B}$	$F=AB$ PLUS A	$F=AB$ PLUS A PLUS 1	$F=A+\overline{B}$	$F=(A+B)$ PLUS A	$F=(A+B)$ PLUS A PLUS 1
H	H	H	L	$F=AB$	$F=AB$ PLUS A	$F=AB$ PLUS A PLUS 1	$F=A+B$	$F=(A+\overline{B})$ PLUS A	$F=(A+\overline{B})$ PLUS A PLUS 1
H	H	H	H	$F=A$	$F=A$	$F=A$ PLUS 1	$F=A$	$F=A$ MINUS 1	$F=A$

Table 9-1-1 Function table of the 74181

The 74181 has two 4-bit inputs A and B, as well as a "carry-in" (CA) input. The purpose of CA is to provide a reverse carry signal (CA=0 when there is a carry). There is a mode control input (M) and 4 function-select lines S0, S1, S2, S3, forming sixteen logic or arithmetic operations.

The 74181 also has a 4-bit output (F3-F0), a "carry-out" or "Cn+4" output; G (Generate) and P (Propagate) output. Refer to the truth table of the 74181 in Table 9-1-1.

The "+" symbol means OR logic, "Plus" means the sum of inputs. The major advantage of the 74181 is its ability to perform arithmetic functions such as addition; subtraction; shifting; and logic functions such as AND, OR and XOR functions.

The mode control input (M) and function-select lines (S0-S3) determines which function it will perform.

The mode control for 74181 is determined by these factors:

1. Addition: A "0" is generated at CA input to signify the existence of a carry. After the arithmetic operation, if the sum is larger than 15, "0" will be generated at CA again.

2. Subtraction: A "0" is generated at Cn+4 if the result is "0" or positive. If "0" is generated at CA, the result is negative or there is a borrow. If the result of subtraction is negative, for example "-4", the 4-bit output F will be in 2's complement and Cn+4=1.

PROCEDURE

1. Set the KL-26005 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block b. Connect function-select lines S3-S0 to Data Switches SW7- SW4 respectively. Connect M to SW3 for selecting arithmetic or logic operation. When M="0" arithmetic operation is performed. When M="1" logic function is performed.

2. Connect inputs A3-A0 to D7-D4 and B3-B0 to D3-D0; Connect Cn to "0"; outputs F3-F0 to Logic Indicators L4-L1 and Cn+4 to L8. Inputs A3-A0, B3-B0 and outputs F3-F0 are active low.
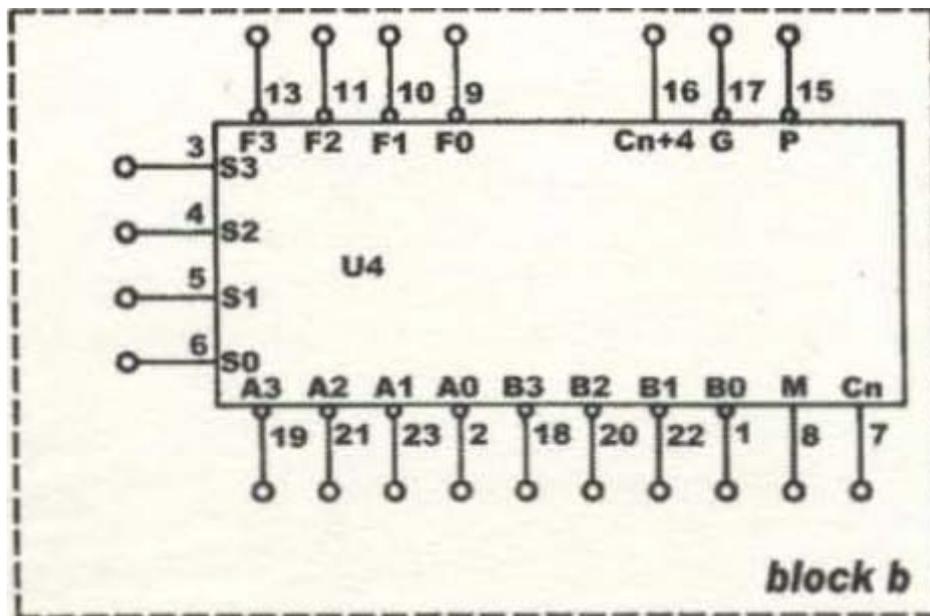

Fig. 9-1-3 Wring diagram (KL-26005 block b, U4=74181)

3. Set M to "1" to perform the following logic functions:

(1) When S3S2S1S0= 0000, A3A2A1A0=0000 and B3B2B1B0=1111, the outputs F3F2F1F0= _____.

(2) When S3S2S1S0= 0000, A3A2A1A0=1100 and B3B2B1B0=1010, the outputs F3F2F1F0=_____.

(3) When S3S2S1S0=1001, A3A2A1A0=1100 and B3B2B1B0=0110, the outputs F3F2F1 F0= _____.

What is the relationship between the inputs and outputs in terms of logic?
_____.

(4) When S3S2S1S0=1011, A3A2A1A0=0011 and B3B2B1B0=1001, the outputs F3F2F1 F0=_____ .

What is the relationship between the inputs and outputs in terms of logic?
_____.

4. Set M to "0", Cn to "0" and ignore the previous carry. Perform the following arithmetic functions:

(1) When S3S2S1S0=1001, A3A2A1A0=B3B2B1B0=0100, the outputs F3F2F1 F0 =_____ and Cn+4 = _____.

(2) When S3S2S1S0=1001, A3A2A1A0=1000 and B3B2B1B0=1100, the outputs F3F2F1F0 =_____ and Cn+4 = _____.

(3) When S3S2S1S0=0011, A3A2A1A0=0100 and B3B2B1B0=0010, the outputs F3F2F1 F0 =_____ and Cn+4 =_____.

(4) When S3S2S1S0=0011, A3A2A1A0=1010 and B3B2B1B0=1000, the outputs F3F2F1 F0 =_____ and Cn+4 =_____.

(5) When S3S2S1S0=0000, A3A2A1A0=1010 and B3B2B1B0=0011 , the outputs F3F2F1 F0 =_____ and Cn+4 =_____.

5. Set M to "0" and Cn to "1", follow the input sequences in Table 9-1-2 and record the outputs. Depending on the state of M and Cn, function-select line S0-S3 has different functions. Refer to the function table of 74181 (Table 9-1-1).

m=0 Cn=1				INPUTS								OUTPUTS				
S3	S2	S1	S0	B3	B2	B1	B0	A3	A2	A1	A0	Cn+4	F3	F2	F1	F0
0	0	0	0	0	0	0	1	0	0	0	1					
0	0	0	0	0	0	1	0	0	0	1	1					
0	0	1	1	0	0	0	1	0	0	1	0					
0	0	1	1	0	1	0	0	0	1	1	0					
0	1	1	0	0	1	0	1	0	1	0	0					
0	1	1	0	0	0	0	1	0	0	1	0					
0	1	1	1	0	1	1	0	0	1	0	1					
0	1	1	1	0	1	1	1	1	0	0	0					
1	0	1	1	1	0	0	0	1	0	0	0					
1	0	1	1	1	1	0	0	0	1	1	0					
1	1	1	1	0	1	1	0	0	1	1	1					
1	1	1	1	0	1	0	1	0	1	1	0					

Table 9-1-2

9-2 Parity Generator Circuit

DISCUSSION

A parity bit, generated by the parity generator, usually accompanies the data transmission process. The parity bit provides as a reference point and allows us to compare and check whether the transmission process and the data transmitted are correct or not.

There are two types of parity generators. The "Odd" parity generator will generate a "1" if the data contains an even number of "1"s. For example, data "10111011" has six "1"s. When the parity bit is added to the end of this data, the number of "1"s in the data will become an "Odd" number, hence the name "Odd Parity Generator",

On the other hand, an Even parity generator will add a "1" to data with odd number of "1"s to make the total number of "1"s even. If the data already has an even number of "1"s no parity bit is generated. Output Y of the Even parity generator shown in Fig. 9-2-1 will be 0 if the inputs ABCDEFGH is equal to 10111011.
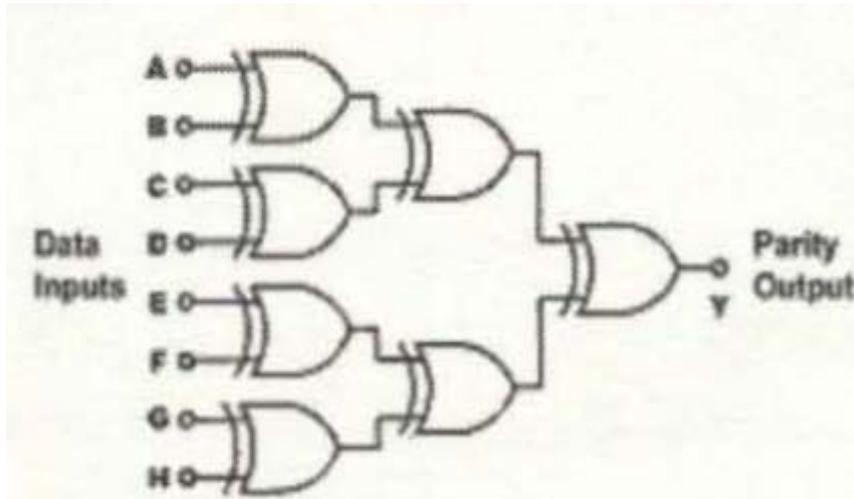
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Fig. 9-2-1 Even parity generator circuit

PROCEDURE

A. Parity Generator Constructed with XOR Gates

1. Set the KL-26002 Module on the KL-22001 Basic Electricity Circuit lab, and locate block a. Complete the connection by referring to the wiring diagram in Fig. 9-2-2 and the even parity generator circuit in Fig. 9-2-3. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26002 Module.
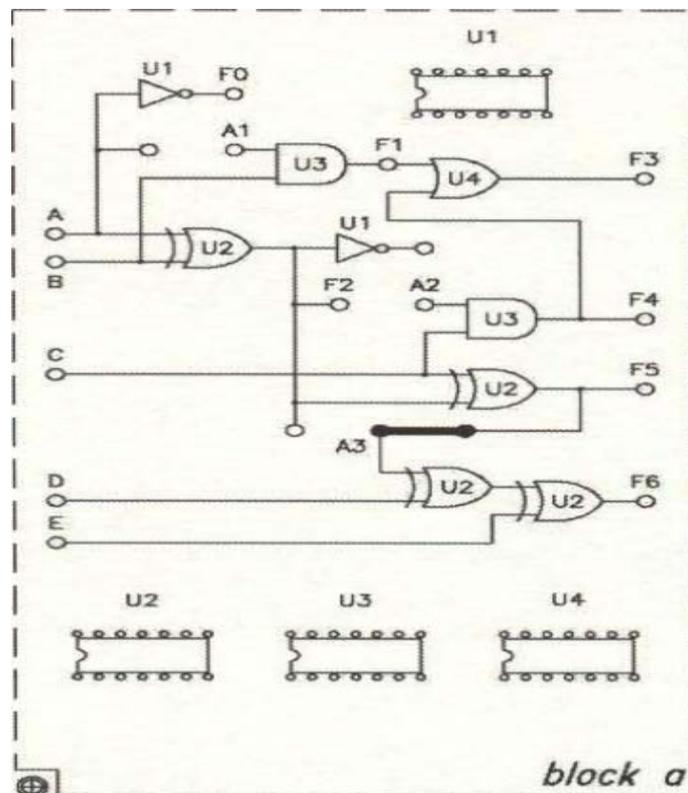

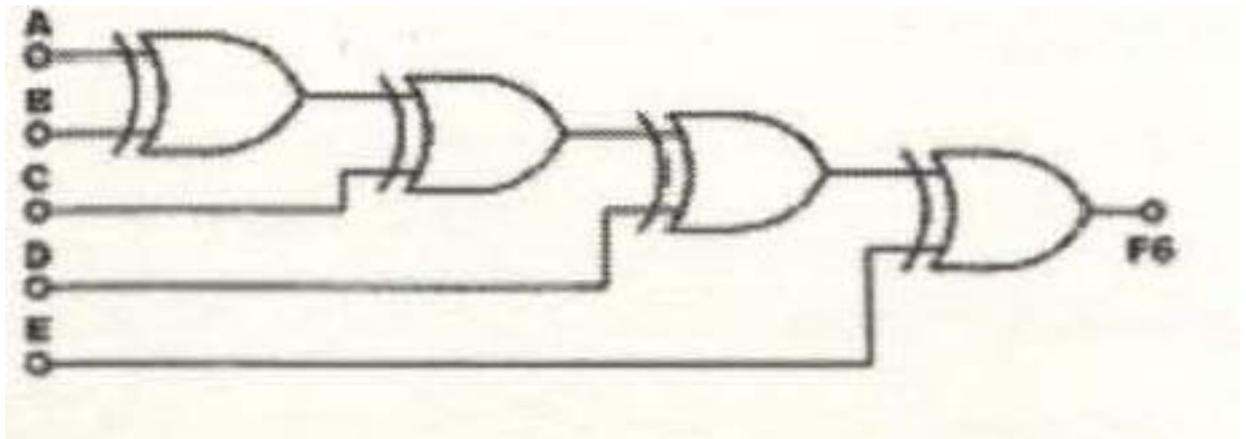Fig. 9-2-2 Wiring diagram (KL-26002 block a)

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Fig. 9-2-3 Even parity generator circuit

2. Connect inputs A, B, C, D, and E to Data Switches SW0-SW4 and output F6 to logic Indicator L1. Follow the input sequences in Table 9-2-1 and record the outputs.

INPUT					OUTPUT
E	D	C	B	A	F6
0	0	0	0	0	
0	0	0	1	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	0	1	
0	1	1	1	0	
1	1	0	0	0	
1	1	0	1	0	
1	1	1	1	0	
1	1	1	1	1	

Table 9-2-1

B. Parity Generator Ic

1. Set the KL-26005 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block c. U7 is a parity generator IC.

2. Connect inputs A1, B1, C1, D1, E1. F1, G1. H1. 11 to Data Switches SW0-SW7 and D7 respectively. Connect outputs Y0 to L1 and Y1 to L2. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26002 Module.
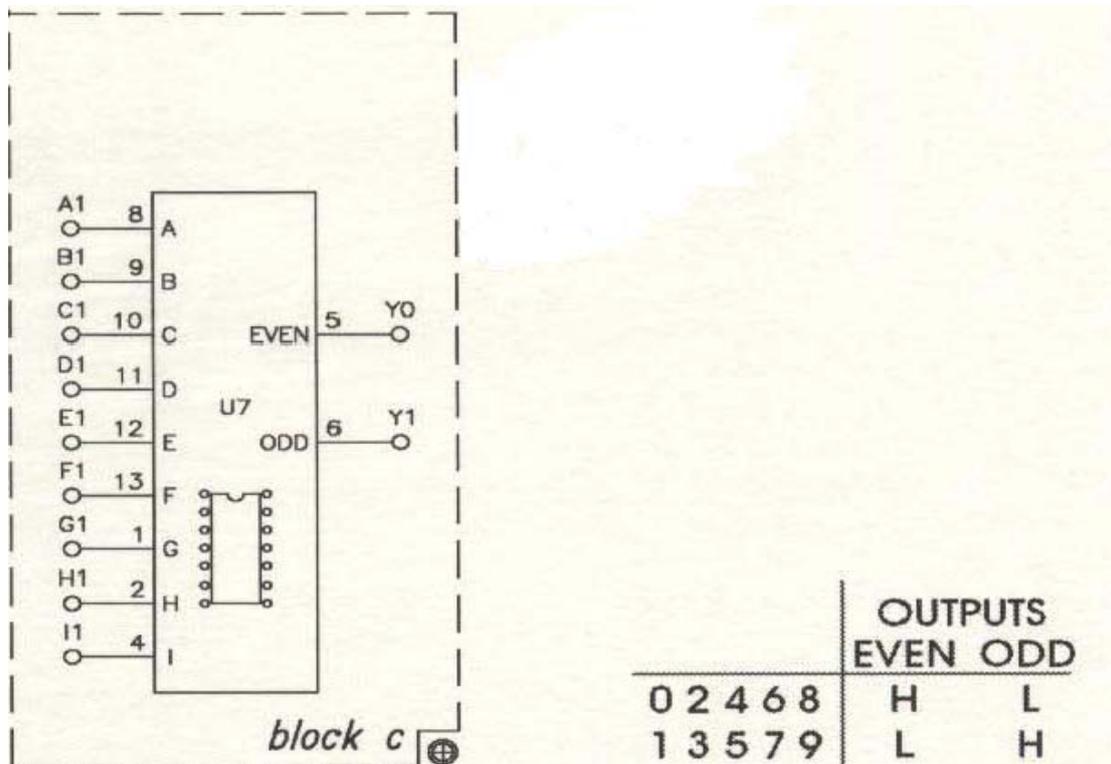

Fig. 9-2-4 Wiring diagram (KL-26005 block c)

3. Follow the input sequences given in Table 9-2-2 and record the outputs.

Inputs									Y0	Y1
L	H	G	F	E	D	C	B	A	(Even)	(Odd)
0	0	0	0	0	0	0	0	0		
0	0	0	0	0	0	0	0	1		
0	0	0	0	0	0	0	1	1		
0	0	0	0	0	0	1	1	1		
0	0	0	0	0	1	1	1	1		
0	0	0	0	1	1	1	1	1		
0	0	0	1	1	1	1	1	1		
0	0	1	1	1	1	1	1	1		
0	1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	0	1		
1	1	1	1	1	1	1	0	0		
1	1	0	0	0	1	1	0	0		

Table 9-2-2

CONCLUSION

1. The 74181 has 16 arithmetic functions with or without carry, at the same time it is also capable of performing various logic functions. Due to time limitation we did not explore each and every function of the 74181. Such a complicated device is not easy to use unless it is controlled by a computer or a microprocessor.

2. Parity generators can be constructed with XOR gates.

3. There are two types of partly generators: Odd and Even.