Bir zeit University

Faculty of Information Technology
Computer Systems Engineering Department

Digital Lab ENCS 211 EXP. No. 3

Encoders, Decoders, Multiplexers and Demultiplexers

3.1 OBJECTIVES

- To understand the operating principles of Encoders/Decoders
- To understand the operating principles of Multiplexers/Demultiplexers
- To construct encoders and decoders using basic gates and IC.
- To construct multiplexers and demultiplexers using basic gates and IC

3.2 EQUIPMENT REQUIRED

1. KL-22001 Basic Electricity Circuit Lab
2. KL-26002 Combinational Logic Circuit Experiment Module (2)
3. KL-26003 Combinational Logic Circuit Experiment Module (3)
4. KL-26004 Combinational Logic Circuit Experiment Module (4)
5. Multimeter

3.3 Theory

3.3.1 Encoder circuit

An encoder is a combinational logic gate that accepts one or multiple inputs and generates a specific output code. Only one input is triggered at a time. An encoder with n-bit inputs and m-bit outputs is shown in Figure.1. When one of the inputs is triggered there will be an m bit output code at the outputs.

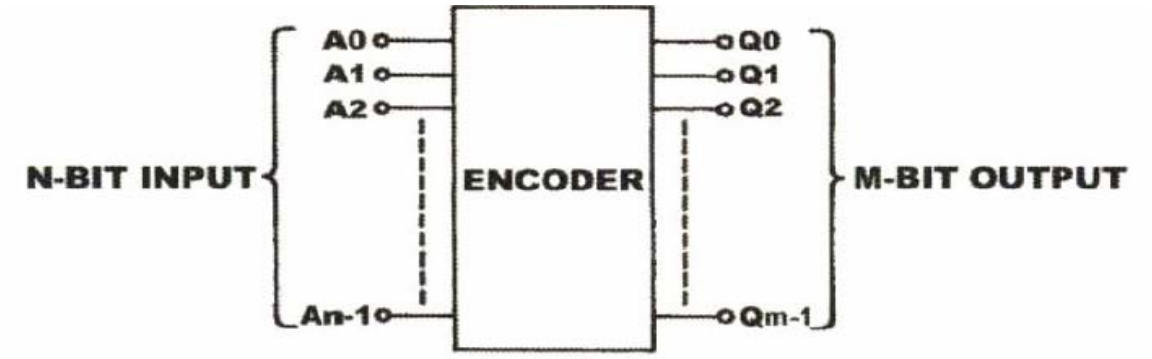

Figure.1: N-to-M Encoder

3.3.1.1 Octal to Binary Encoder

An octal to binary encoder is shown in Figure.2. There are 8 octal inputs A1-A7 (0-7); and three binary outputs Q0, Q1 and Q2 (000-111). If input A0="0", the corresponding output Q2Q1Q0 is equal to "000".

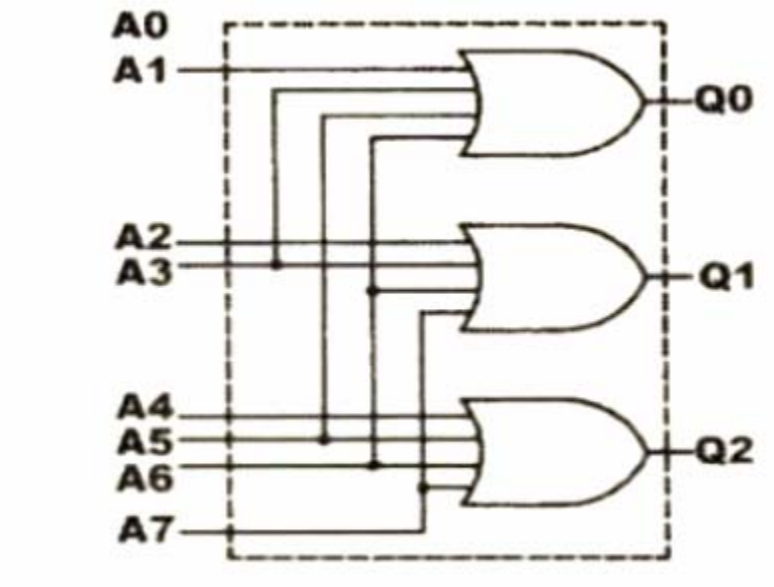

Figure.2: Octal-to-Binary Encoder

Actually, A0 is not connected to the gate input. If A1="1" then Q2Q1Q0=001.
When A2="1" the output Q2Q1Q0=010. There can't be more than one "1" among the inputs. For example, if A2="1" and A3="1" simultaneously, Q2Q1Q0=011. If A3, A4 both are "1" at the same time, Q2Q1Q0=111. Both outputs are incorrect.

3.3.1.2 10-to-4 line priority Encoder (74147)

The 74147 is a 10-t0-4-line priority BCD output encoder, the input priority runs in ascending order, gate 1 has the lowest and gate 9 has the highest priority. The outputs are in BCD code. Table.1 is the function table for the 74147 10-to-4- line decimal-to-BCD priority encoder. It encodes nine data lines to four-line BCD.
The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level.

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	B	C	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Table.1: 74147 Function Table

Both input and output of the 74147 are active low. When inputs 1-9 are all at a high state, output DCBA="HHHH". When inputs 2 and 5 are active simultaneously the output is determined by input 5, which has higher priority than input 2. When inputs 2, 5 and 7 are active together, input 7 will determine the output.

3.3.2 Decoder Circuits

A decoder is a logic circuit that will detect the presence of a specific binary number or word. The input to the decoder is a parallel binary number and the output is a binary signal that indicates the presence or absence of that specific number.

The AND gate can be used as a basic decoder circuit, since the AND gate output will be a binary 1 only when all inputs are binary 1. Proper connections of AND gate inputs to the data will ensure detection of any binary number.

3.3.2.1 Binary-to Octal Decoder

A binary-to-octal decoder is shown in Figure.3. There are 3 binary inputs A, B, C and 8 octal outputs Q0-Q7. If CBA="010", the output Q2="1". When CBA="111", the output Q7="1".

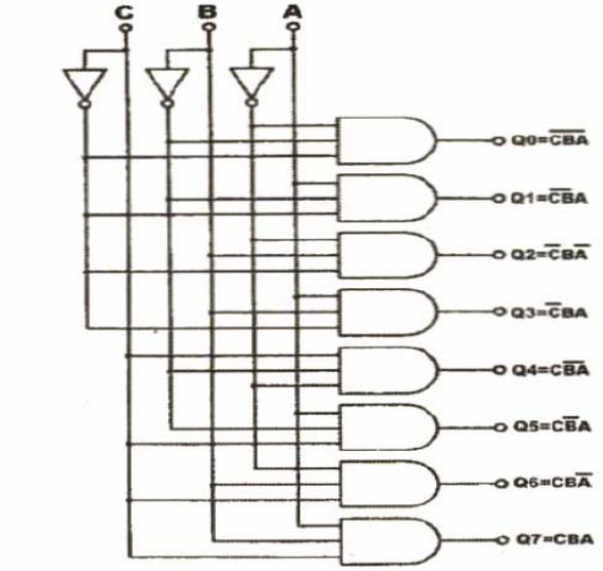

Figure.3: Binary-to-Octal Decoder

3.3.3 Multiplexer Circuits

Multiplexer, or MUX, is a logic circuit that select and rout any number of inputs to a single output. One of the multiple inputs is selected by the selector gates and is routed to the single output. The number of selector gates determined the capacity of a multiplexer. For example, if a certain MUX has only one selector gate (Figure.4), it is referred to as a “2-to-1 line MUX” because one selector can only select from two inputs.

A MUX with 3 selector gates is called “8-to-1 line MUX”, since 3 selectors are capable of selecting an output from 8 inputs. MUX is also referred to as “Data Selector” because it selects one output from among many inputs.

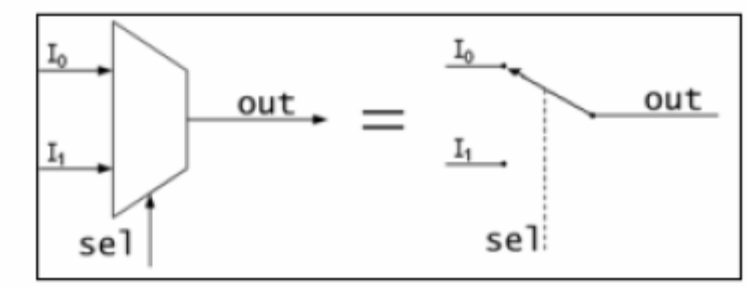

Figure.4: schematic of 2-to-1 MUX

3.3.4 Demultiplexer Circuits

A demultiplexer, or DMUX, is basically a logic circuit that is opposite of a multiplexer. DMUX has a single input and multiple outputs. The input can be connected to any one of the many outputs through the selector terminal. The
DMUX is referred to as "Data Distributor" or "Data Router". Its pin assignment diagram is shown in Figure.5 (a).

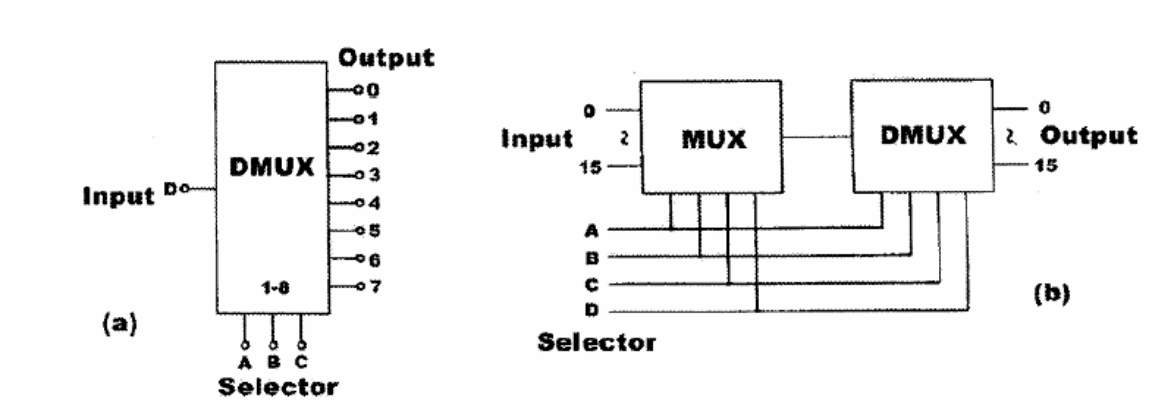

Figure.5: Demultiplexer Circuits

When all the selector terminals A, B and C are in low logic state (CBA=000), data at input D is send to output number 0. When CBA=010, the input is send to output number 2. Collective state of selectors determines the location of output data. When CBA=111, data is send to the last output (output number 7). By combining MUX and DMUX, long distance transmission systems can be set up, increasing the efficiency of transmission lines. Figure.5 (b) shows a MUX-DMUX combinational circuit with 16 inputs, 16 outputs and 4 selectors.

3.4 Pre-Lab

1. Prepare all sections and Hand out all the required designs to your teaching assistant.

2. Design, construct, and test a circuit which uses an SN74151 to implement a sum-of-products expression.

(a) Convert the following expression into summation form (i.e. F(A,B,C)= ∑(…)):

$$Y = f(A,B,C) = A\overline{B} + \overline{B}C$$

(b) Sketch on figure.6 the input connections necessary to implement the function in **a**

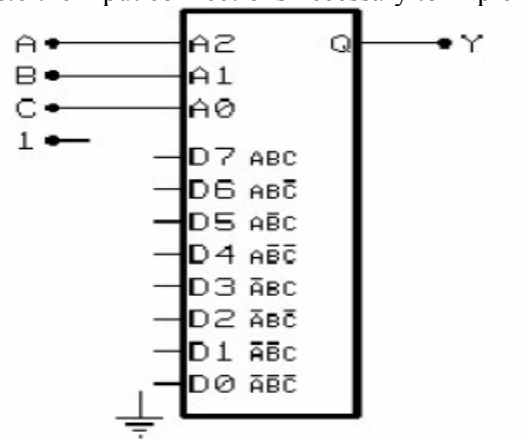

Figure.6: 8-to-1 Multiplexer

(c) Refer to function in (a) to fill in the table bellow (table.2)

INPUTS A	B	C	OUTPUT Y	Y'
L	L	L		
L	L	H		
L	H	L		
L	H	H		
H	L	L		
H	L	H		
H	H	L		
H	H	H		

Table.2

3. Design, construct, and test a circuit which uses an SN74138 demultiplexer to implement a sum-of-products expression.

(a) Convert the following expression into summation form (i.e. F(A,B,C)= ∑(…)):

$$Y = f(A, B, C) = \overline{A}BC + B\overline{C}$$

(b) The demultiplexer output is selected, and will go low, by the address on inputs A, B, and C when the IC is enabled. Therefore, we can create the output function Y by summing together the outputs indicated by the summation form of Expression 1.2. Since the outputs of the demultiplexer are active- low, this is done with a NAND gate. Connect each of the TRUE minterm outputs of the demultiplexer in Figure.7 (indicated by the summation equation) to an input of the NAND gate. Connect all unused NAND inputs to logic 1.

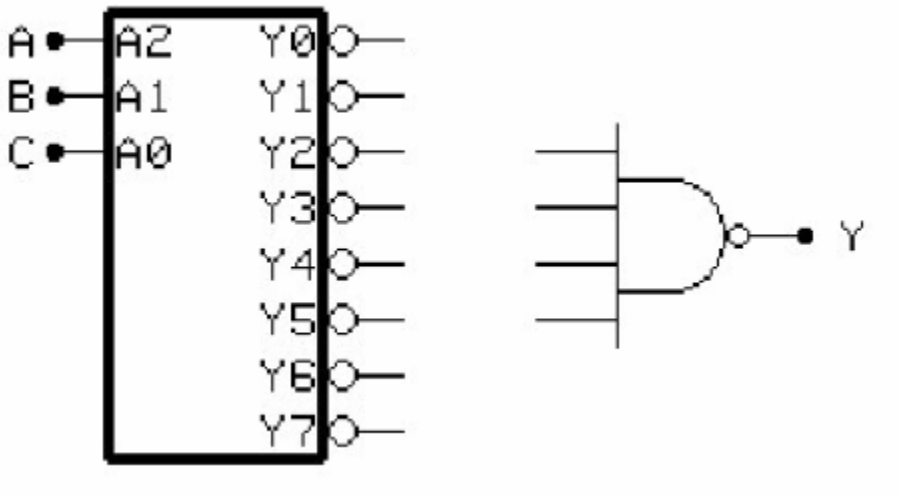

Figure.7: 3-to-8 DeMUX

3.5 Procedure:

A. Constructing 4-to-2-Line Encoder with Basic Gates

1. Set the KL-26003 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block a. Complete the connections by referring to the wiring diagram in Figure.8

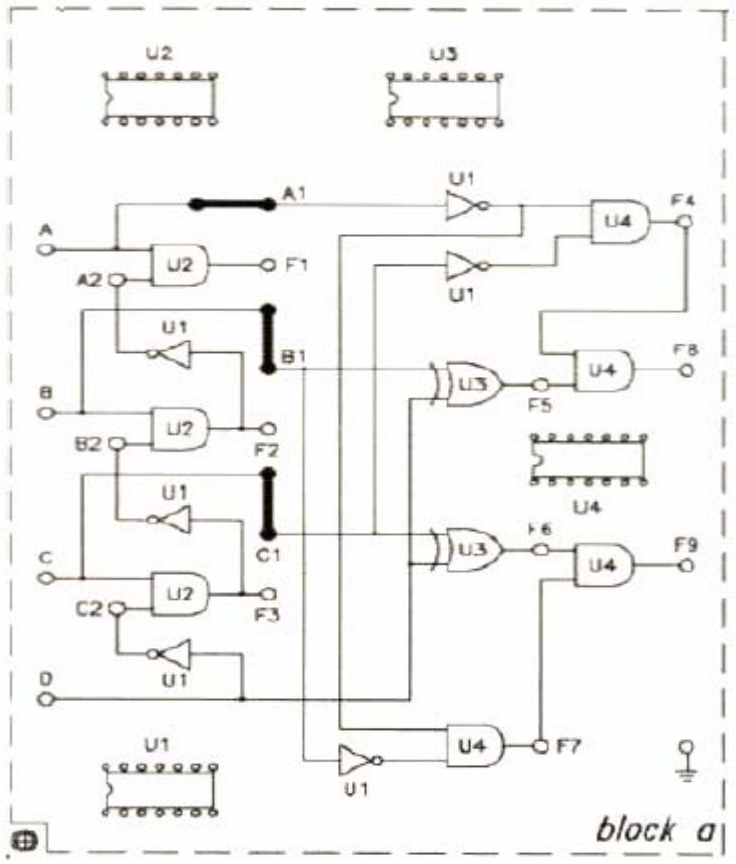

Figure.8: wiring diagram of 4-to-2 line Encoder

2. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL-26003 Module.
3. Connect inputs A-D to Data Switches SW0-SW3 respectively; outputs F8 and F9 to Logic Indicator L0 and L1.
4. Follow the input sequences for D, C, B, A in Table. 3 and record the output states.

D	C	B	A	F9	F8
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Table.3

B. Constructing 4-to -2 priority encoder

Given the 4-to-2 priority encoder of Figure.8, implement this circuit using **NAND gates only.** Then follow the input sequence of Table.4. Note that input D0 is disconnected

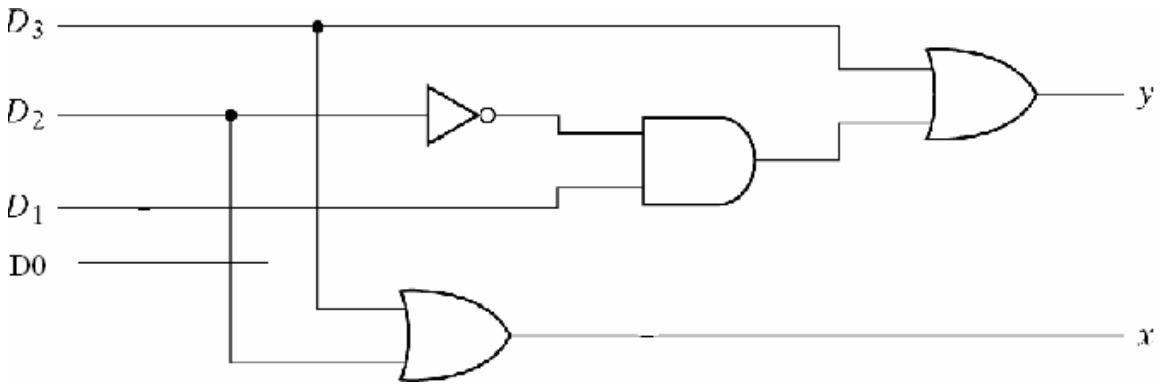

Figure.8: 4-to-2 Priority Encoder

D0	D1	D2	D3	X	Y
0	**0**	**0**	**0**		
0	**0**	**0**	**1**		
0	**0**	**1**	**0**		
0	**0**	**1**	**1**		
0	**1**	**0**	**0**		
0	**1**	**0**	**1**		
0	**1**	**1**	**0**		
0	**1**	**1**	**1**		
1	**0**	**0**	**0**		
1	**0**	**0**	**1**		
1	**0**	**1**	**0**		
1	**0**	**1**	**1**		
1	**1**	**0**	**0**		
1	**1**	**0**	**1**		
1	**1**	**1**	**0**		
1	**1**	**0**	**1**		

Table.4

C. Constructing 10-to-4-Line Encoder with TTL IC

Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block a. The 74147 (U7l) decimal to BCD priority encoder in Figure.9 will be used in the following steps.

1. Apply +5 VDC from Fixed Power to KL-26004.
2. Connect inputs A1-A8 to SW0-SW7, A9 to D7. Connect outputs F1-F4 to Logic indicators L1-L4. Follow the input sequences given in Table.5 and record output states.

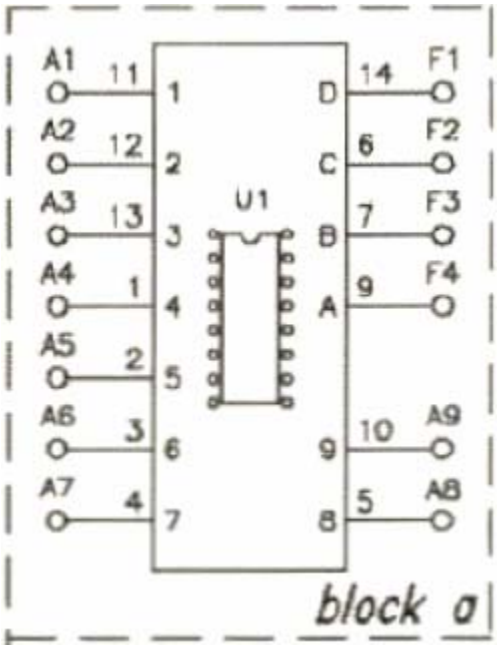

Figure.8 :(74147)BCD Priority Encoder

A9	A8	A7	A6	A5	A4	A3	A2	A1	F4	F3	F2	F1
0	1	1	1	1	1	1	1	1				
0	0	1	1	1	1	1	1	1				
1	1	1	1	1	1	1	1	0				
1	1	1	1	1	1	1	0	0				
1	1	1	1	1	1	0	1	1				
1	1	1	1	1	0	0	0	0				
1	1	1	1	0	1	1	1	1				
1	1	1	1	0	0	0	1	1				
1	1	1	0	1	1	1	0	0				
1	1	0	1	1	0	1	1	0				
1	1	0	0	0	1	1	1	1				
1	0	0	0	0	0	1	1	1				

Table.5

D. Constructing 2-to4-Line Decoder with Basic Gates

1. Set the KL-26003 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block c. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL-26003 Module.

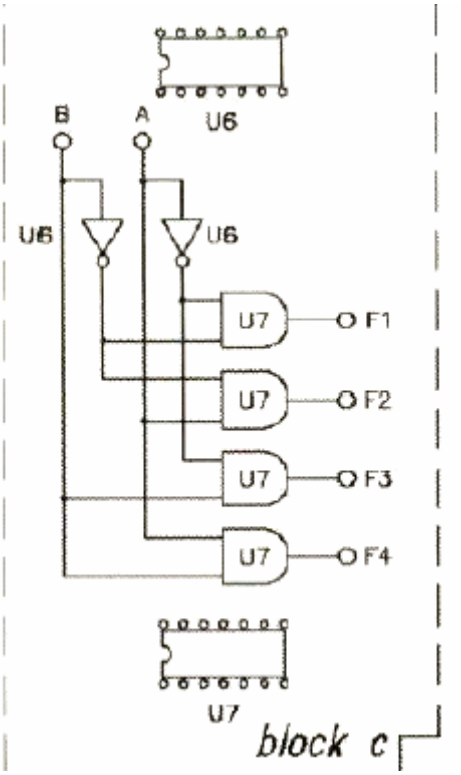

Figure.9: 2-to-4 Decoder (KL_26003 block C)

2. Connect inputs A and B to Data Switches SW0 and SW1. Connect outputs 1-F4 to Logic Indicators L0-L3 respectively.

3. Follow the input sequences for A and B in Table.6 and record output states

B	A	F1	F2	F3	F4
0	0				
0	1				
1	0				
1	1				

Table.6

E. Constructing 4-to-10-Line Decoder with TTL IC

1. Set the KL-26002 module on the Kl-22001 Basic Electricity Circuit Lab, and locate block c. U10, 7442 4-to-10-line (or BCD to Decimal) decoder will be used in the following steps.

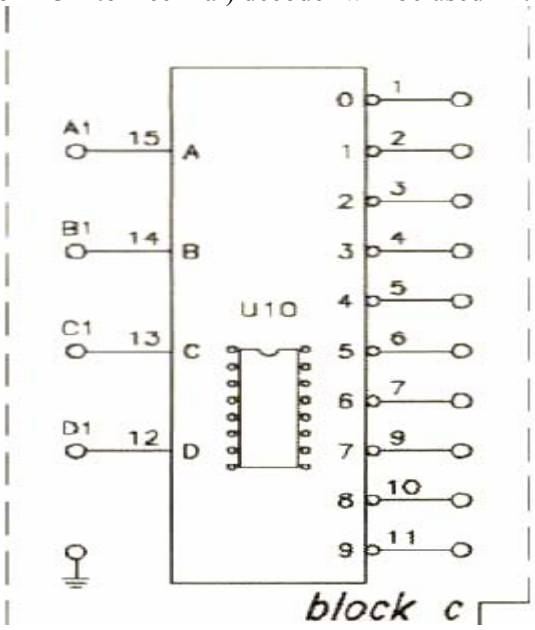

Figure.10: 4-to-10 line Decoder

2. Connect inputs A1, B1, C1, D1 to the Data Switches SW0, SW1, SW2, and SW3, respectively. Connect outputs 0-9 to Logic Indicator Lo-L9. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL-26002 Module.

3. Follow the input sequences for A- D in Table.7 and record output states.

BCD	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0									
1	0	0	0	1	1									
2	0	0	1	0	1									
3	0	0	1	1	1									
4	0	1	0	0	1									
5	0	1	0	1	1									
6	0	1	1	0	1									
7	0	1	1	1	1									
8	1	0	0	0	1									
9	1	0	0	1	1									

Table.7

F. Constructing BCD-to-7-Segment Decoder

1. Set the KL-26003 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block b. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL-26003 Module. The U5 7448 is a BCD-to-7-segment decoder/driver with internal pull-up outputs.

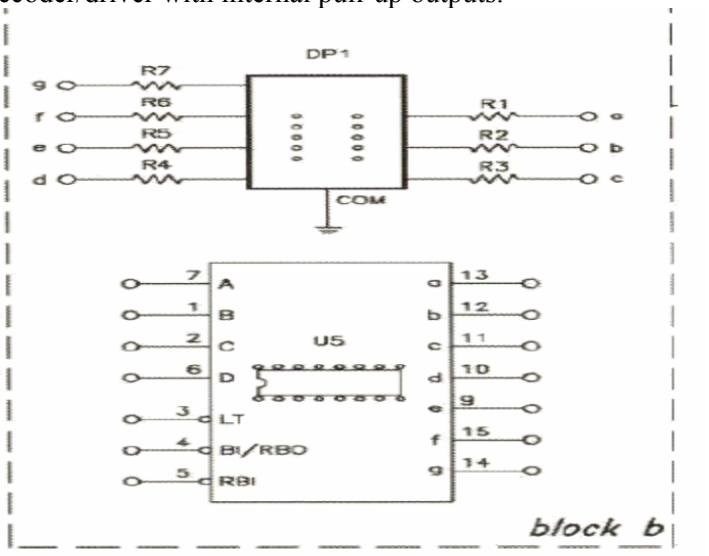

Figure.11: Wiring diagram (KL-26003 block b)

2. Connect BCD inputs D, C, B, A to Data Switches SW3, SW2, SW1, SW0, respectively. Connect decoder outputs a - g to DP1 inputs a – g respectively Connect "RBI" to SW7, "LT" to SW6, and "BI/RBO" to Logic Indicator L0.

3. Set RBI= "1" and LT="1". Follow the input sequences for D, C, B, A in Table.8 and record outputs of the 7-segment display DP1.

4. Set LT="0". Observe and record the display on DP1.

D	C	B	A	Display Pattern
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	1	

Table.8

5. Set RBI="0" and LT="1". Observe and record the display on DP1.

G. Constructing 2-to-1-Line Multiplexer with basic Gates

1. Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block e. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL- 26004 Module.

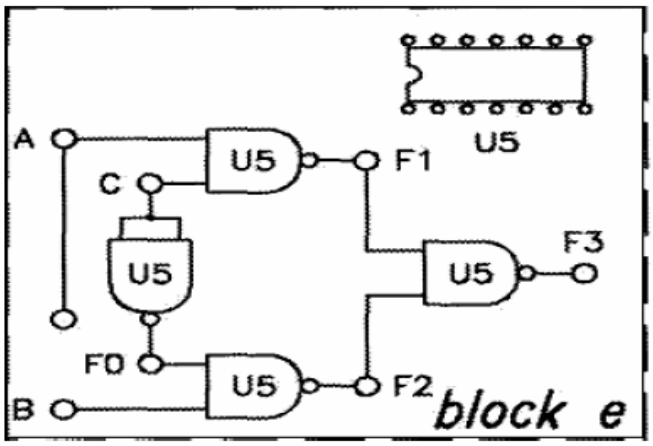

Figure.12: 2-to-1 Multiplexer

2. Connect inputs A, B to Data Switches SW0, SW1; selector C to SW2. Connect Output F3 to Logic Indicator L0.

3. Follow the input sequences in Table.9 and record states of F3.

Which input (A or B) determines the output when C=O? _____
Which input (A or B) determines the output when C=1? _____

C	B	A	F3
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table.9

H. Using Multiplexer to Create Function

1. Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block f. Apply +5 VDC from the Fixed Power on KL-22001 Lab to KL-26004 Module

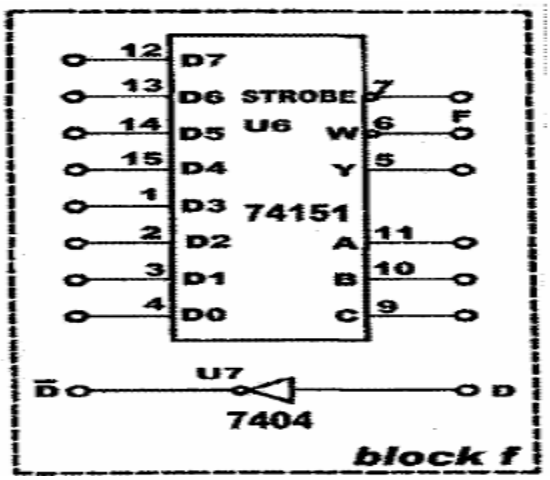

Figure.13: Wiring diagram (KL-26004 block f)

2. The U6 (74151) will used to create the function:
F (D, C, B, A) =∑(0,2,4,5,7,8,10,11,15) 3. Sketch on (**Figure.13**) the input connections necessary to implement the function

F (D, C, B, A) =∑(0,2,4,5,7,8,10,11,15).

4. Complete the connection by referring to the wiring diagram in Figure.13

5. Connect inputs D, C, B, A to Data Switches SW3, SW2, SW1, SW0 respectively. Connect output Y to Logic Indicator L0. Follow the input sequences in Table.10 and record output states.

D	C	B	A	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Table.10

I. Constructing 8-to-1-Line Multiplexer with TTL IC

1. Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block f. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26004 Module.

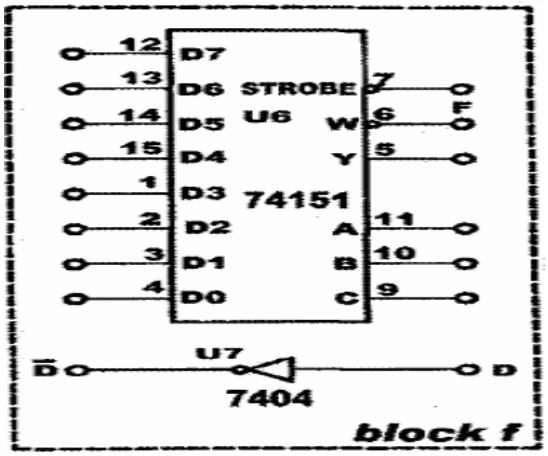

Figure.14: 8-to-1 MUX (KL-26004 block f)

2. Refer to the data sheet for specifications of the 74151, U6
When CBA ="000", data at D0 is send to output *Y*.
When CBA ="010", data at D2 is send to output Y.
When CBA ="111", data at D7 is send to output Y.
The IC will function properly only when STROBE ="0".
Y will remain “0” when STOROBE=”1”.

3. Connect inputs D0~D7 to Data Switches D0~D7; input C, B, A to Data Switches SW2, SW1, SW0. Connect STROBE to Data Switch SW3. Connect output Y and F to Logic Indicators L0 and L1, respectively. Set SW3 to "0". Follow the input sequences in Table.11, switch D0~D7 and record output states. Determine on which input among DO~D7 does Y depend on.

C	B	A	Y	F
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table.11

J. Constructing 1-to-2-Line Demultiplexer with Basic Logic Gates

1. Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block e. Complete the connection by referring to the wiring diagram in Figure.15.Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26004 Module.

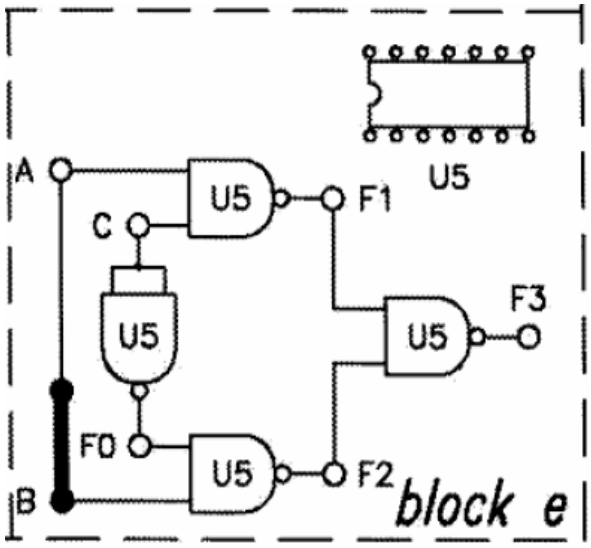

Figure.15: 1-to-2 Demultiplexer

2. Connect A to Data Switch SW0; C to SW3; F1 and F2 to Logic Indicators L0and L1 respectively.

3. Set C to "1", change A and observe outputs F1 and F2._____

4. Set C to "1", change A and observe outputs F1 and F2. _____

K. Constructing 1-to-8-Line Demultiplexer with CMOS IC

1. Set the KL-26004 Module on the KL-22001 Basic Electricity Circuit Lab, and locate block b as shown in Fig 1.8. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26004 Module. U2 (4051) will be used in the experiment.

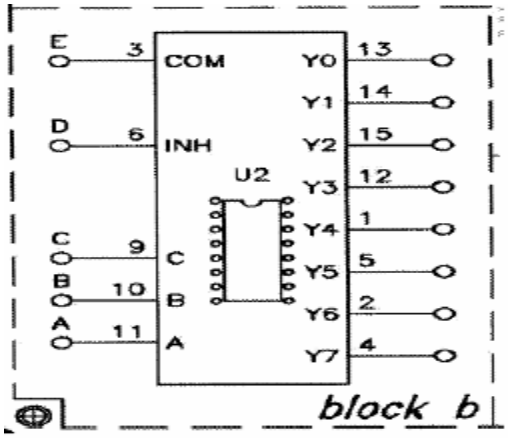

Figure.16: 1-to-8 Demultiplexer

2. Connect E and D to Data Switches D0 and D1, respectively. Connect input A to SW0, B to SW1, C to SW2; outputs Y0~Y7 to Logic Indicators L0~L7, respectively.
3. Set D=”0”, apply the sequence 1-0-1-0 to the Common Input E and observe output Y0~Y7.Do the outputs change as the input sequence is?_____.

4. Set D="1", apply the input sequence 1-0-1-0 to the Common Input E and observe outputs Y0~Y7. Do the outputs change as the input sequence is applied? _____
Which state of D changes the outputs? _____

5. Set D="0". Using the same sequence for E (1-0-1-0), follow the sequence for A, B and C given in Table.12. Record output states.

C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

Table.12

3.6 PROBLEM
Design a Majority Circuit; A circuit that takes 4 inputs and outputs 1 output, its output equals 1when 3 or 4 of the inputs are 1. ***You can only use two 4×1 multiplexers.***