**Theory:**

**1. Compartor circuit:**

Comparator is an combinational logical circuit that constructed from basic gates AND, OR…etc. This circuit perform comparison between at least two number and the output determine which the number is greater or equal to another number by generate 0,1.

**2. Adder circuits:**

**A-Half Adder circuit:**

A Half adder is a combinational logical circuit and that constructed from basic gates AND ,OR,…etc ,and that performs an addition operation on two binary digits. The half adder generate two values the first value is a sum and the second value is a carry ,which are both binary digits.

**B-Full Adder circuit:**

A FULL adder is a combinational logical circuit and that constructed from basic gates AND ,OR,…etc also we can construct a Full Adder from two half adders,and that performs an addition operation on three binary digits one of them is a previous carry. The half adder generate two values the first value is a sum and the second value is a carry ,which are both binary digits.

**3. Subtractor circuits:**

**A-Half-Subtractor**

A Half‐subtractor is a circuit that performs a subtraction of two 1‐bits. This kind of circuits doesn’t take “Borrow” from previous subtractions under consideration and generate two output the first value is the result of subtraction and the second value is the borrow, This binary subtraction is performed by using 2’s complement. The complement is done by two

steps:

• The subtrahend is inverted to 1’s complement.

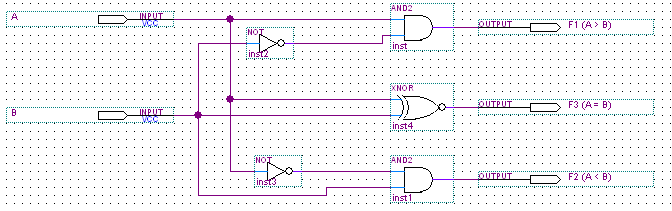
• A “1” is added to the least significant bit of the subtrahend in 1’s complement.

**B-Full-Subtractor**

A Full‐subtractor considers borrow from previous stages , therefore the input pin of the circuit is three on of these inputs is borrow from previous stage ,then generate two output the first value is the subtraction and the second value is the borrow ,the circuit of the full subtractor.

**Procedure :**

1. **Comparator Circuits**
2. **Constructing Comparator with Basic Logic Gates:**

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Fig(1) (basic comparator)

|  |  |  |
| --- | --- | --- |
| INPUT |  | OUTPUT |
| B A |  | F1 F2 F3 |
| 0 0 | A = B | 1 1 0 |
| 0 1 | A > B | 0 1 1 |
| 1 0 | A < B | 1 0 1 |
| 1 1 | A = B | 1 1 0 |

Table(1) (the truth table of the basic comparator)

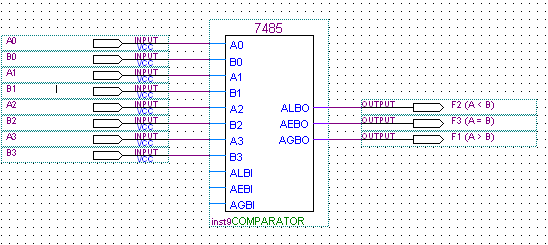
Constructed the circuit in figure (1) by using KL-26001 Module on the KL-22001 Basic Electricity Circuit Lab, and locate **block a**.

connect the input A&B to switch SW1 & SW2 respectively ,then connect the output F1,F2,F3,F4 to led then take the output and record it in table(2).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| B (SW2) | A (SW1) | F1 | F2 | F5 |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

Table (2)

**B- Constructing Comparator with TTL IC** :



Fig(2)(4bit Comparator with TTL IC)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| A3 A2 A1 A0 | A3 A2 A1 A0 | F1 F2 F3 |
| 0 0 0 0 | 0 0 0 0 | 0 0 1 |
| 0 1 0 1 | 0 0 1 1 | 1 0 0 |
| 0 1 0 0 | 1 0 0 0 | 0 1 0 |
| 1 0 1 0 | 1 0 1 0 | 1 0 0 |
| 0 1 1 0 | 1 0 1 1 | 0 1 0 |
| 1 1 1 1 | 1 1 0 0 | 1 0 0 |

Table(3)(truth table of a 4-bit comparator)

The 7485 4-bit comparator IC on KL26005 Module on the KL-22001 Basic Electricity Circuit Lab was used and connected as fig. (2):

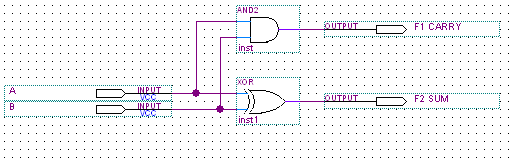
To construct the above circuit connect inputs A1~A4 to SW4 ~ SW7 and B1 ~ B4 to SW0 ~ SW3, Respectively. The outputs A=B were Connected to L1, A<B to L2, and A>B to L3, then record it in table(4).

Table (4)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A4 | A3 | A2 | A1 | B4 | B3 | B2 | B1 | A>B | A<B | A=B |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**2-Half- and Full-Adder Circuits**

1. **Half -Adder with Basic logic Gates:**

****

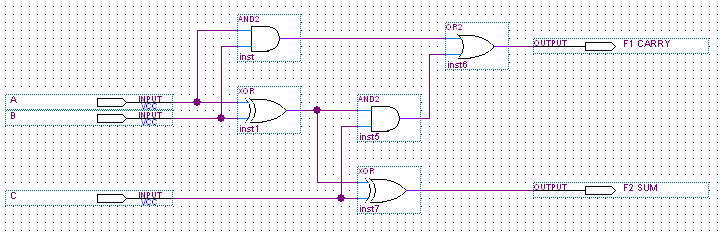
Fig(3) (half adder)

This circuit in fig(3) was connected and the truth table is obtained to be as in table(5) below :

|  |  |
| --- | --- |
| INPUT | OUTPUT |
| B A | F1 © F2(SUM) |
| 0 0 | 0 0 |
| 0 1 | 0 1 |
| 1 0 | 0 1 |
| 1 1 | 1 0 |

Table(5) (truth table for half adder)

1. **full -Adder with Basic logic Gates:**



Fig(4)

|  |  |
| --- | --- |
| INPUT | OUTPUT |
| C B A | F1© F2(SUM) |
| 0 0 0 | 0 0 |
| 0 0 1 | 0 1 |
| 0 1 0 | 0 1 |
| 0 1 1 | 1 0 |
| 1 0 0 | 0 1 |
| 1 0 1 | 1 0 |
| 1 1 0 | 1 0 |
| 1 1 1 | 1 1 |

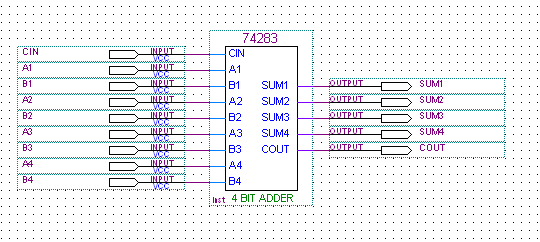
Table(6)

The circuit in fig(4) was connected using the basic logic gates, after that the truth table was obtained to be as in table (6)

1. **4 bit full -Adder with IC :**

With this type of circuits its possible to add to numbers with 4-bit digits each ,The circuit was constructed as shown in fig(5) ,then the truth table was considered in table(7) which explain the result of adding tow 4-bit numbers.

The circuit that considered in the lab as shown in fig(6).



Fig(5)

|  |  |  |  |
| --- | --- | --- | --- |
| Y | X | ∑ | F1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 6 | 6 | 0 |
| 0 | 9 | 9 | 0 |
| 0 | F | F | 0 |
| 1 | 3 | 4 | 0 |
| 1 | 6 | 7 | 0 |
| 1 | 8 | 9 | 0 |
| 3 | 6 | 9 | 0 |
| 4 | 8 | D | 0 |
| 4 | F | 3 | 1 |
| 8 | 7 | F | 0 |
| 9 | 9 | 2 | 1 |
| A | B | 5 | 1 |
| C | E | A | 1 |
| F | F | E | 1 |

Table(7)

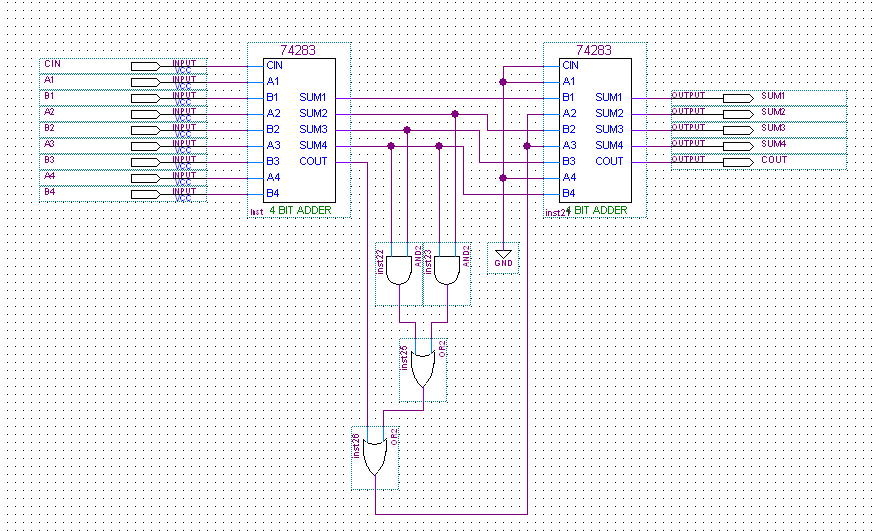


Fig(6)

1. **BCD Adder :**

The inputs and outputs were connected at the circuit in fig(7)

So the truth table will be as in table(8)



Fig(7)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| X3 X2 X1 X0 | Y3 Y2 Y1 Y0 | COUT RESULT |
| 0 0 0 0 | 0 0 0 0 | 0 0000 |
| 0 0 0 1 | 0 0 1 1 | 0 0100 |
| 0 0 1 1 | 0 1 0 0 | 0 0111 |
| 0 0 1 0 | 0 0 1 0 | 0 0100 |
| 0 0 1 0 | 1 0 0 0 | 1 0000 |
| 0 0 1 1 | 0 1 1 0 | 0 0100 |
| 0 1 0 0 | 0 0 1 0 | 0 0110 |
| 0 1 0 0 | 0 1 0 1 | 0 1001 |
| 0 1 0 0 | 0 1 1 0 | 1 0000 |
| 0 1 0 1 | 0 1 1 0 | 1 0001 |
| 0 1 1 0 | 0 1 1 1 | 1 0011 |
| 0 1 1 1 | 1 0 0 0 | 1 0101 |
| 0 1 1 1 | 1 0 0 1 | 1 0110 |
| 1 0 0 0 | 1 0 0 1 | 1 0111 |
| 1 0 0 1 | 1 0 0 1 | 0 1000 |
| 1 0 1 0 | 1 0 1 0 | 0 1010 |
| 1 0 1 0 | 1 0 1 1 | 0 1011 |
| 1 0 1 0 | 1 1 0 0 | 0 1100 |
| 1 0 1 1 | 1 1 1 0 | 0 1111 |
| 1 1 1 1 | 1 1 1 1 | 1 0100 |

Table(8)

1. **Half and full - subtractors :**

this type of circuits is a special case of the adders ;

it convert the neg. number to its equivalent 2's complement formula

and then do the add operation .

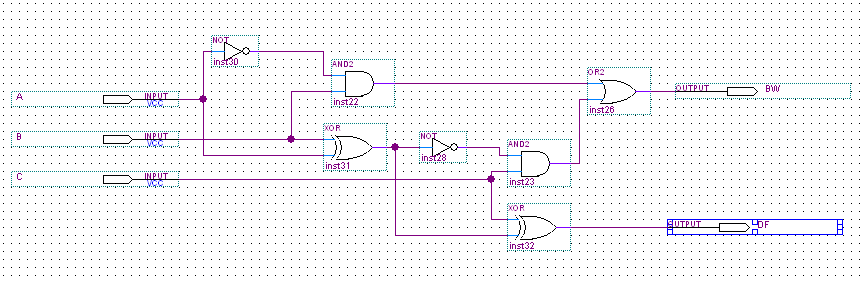
the circuits of half and full subtractors was connected and the truth tables was obtained as shown below .

For half-subtractor

D = | X – Y| B= 1 if Y>X else 0 .

For full-subtractor

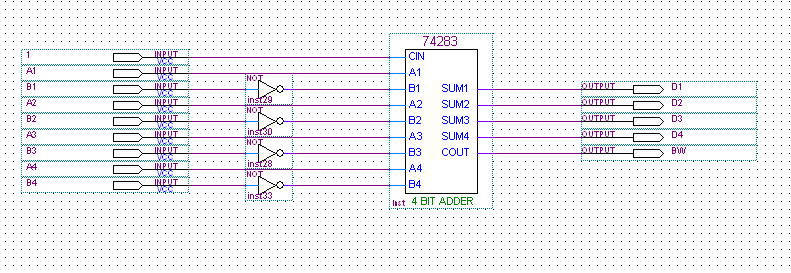
D = | |X – Y| - Bin| B = 1 if X< Y + Bin else 0 .



Fig(8) ( afull- sub using tow half- sub wit basic gates )

|  |  |  |
| --- | --- | --- |
| INPUT | OUTPUT | |
| C A B | BW1 DF1 | BW2 DF2 |
| 0 0 0 | 0 0 | 0 0 |
| 0 0 1 | 1 1 | 1 1 |
| 0 1 0 | 0 1 | 0 1 |
| 0 1 1 | 0 0 | 0 0 |
| 1 0 0 | 0 0 | 1 1 |
| 1 0 1 | 1 1 | 1 0 |
| 1 1 0 | 0 1 | 0 0 |
| 1 1 1 | 0 0 | 1 1 |

Table (9)(truth table for full subtractor)



Fig(9) (4- bit subtractor with IC)



Fig(10) (4- bit subtractor with IC which we dealt with in lab)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| X3 X2 X1 X0 | Y3 Y2 Y1 Y0 | BW DIFFER |
| 0 1 0 0 | 0 1 0 0 | 1 0000 |
| 0 1 0 0 | 0 0 1 1 | 1 0001 |
| 1 0 0 0 | 0 0 1 1 | 1 0101 |
| 1 0 0 0 | 0 0 0 1 | 1 0111 |
| 1 0 0 1 | 1 0 0 0 | 1 0001 |
| 1 0 0 1 | 0 1 1 1 | 1 0010 |
| 1 0 1 0 | 0 1 1 0 | 1 0100 |
| 1 0 1 0 | 0 1 0 1 | 1 0101 |
| 1 0 1 1 | 1 0 1 0 | 1 0001 |
| 1 1 1 1 | 1 0 1 0 | 1 0101 |

Table (10)( truth table for 4- bit subtractor)

**Conclusion:**

In this experiment ,we understand how the Full and Half Adder work and how we can construct it ,also how to build FULL –Adder form two Half -Adder ,therefore we were able to construct 4-bit from Full-Adder, but in this experiment we used an IC and that IC is 4-bit Adder to understand how this adder work ,also we constructed BCD Adder by using two 4-bit Adder and basic gates to Add 6 to original number when the number greater than 9,but we faced a problem and that problem when the number greater than 15 the carry must be shown , but actually not shown. I think that problem that happen since sometimes the current be very small, therefore the carry not shown.

Comparator, in this experiment we understand how 2-bit comparator work ,also how 4-bit comparator work by using IC comparator ,also we faced a problem and that problem is some switches don’t work with comparator ,but actually these switches work normally when we used it in another circuit ,but we solved these problem the change some switches to another switches(D0-D7) ,and I think the switches(sw5 &sw6 &sw7) don’t work properly since sometimes the current in these switches are so small and that cause an error when using 4-bit comparator.

Subtractor,in this experiment we understand how the Half and Full Subractor work ,also how to construct Half-Subtractor from basic gates ,therefore we can able to construct Full-Subtractor from Half-Subtractor . Also we constructed 4-bit Subtractor by using an IC .In this section we didn’t face any problem and all results are accepted as we expected.

Finally , we interested when we do this experiment ,since we learned how the different types of Adders ,Subtractors ,and Comparators are work .

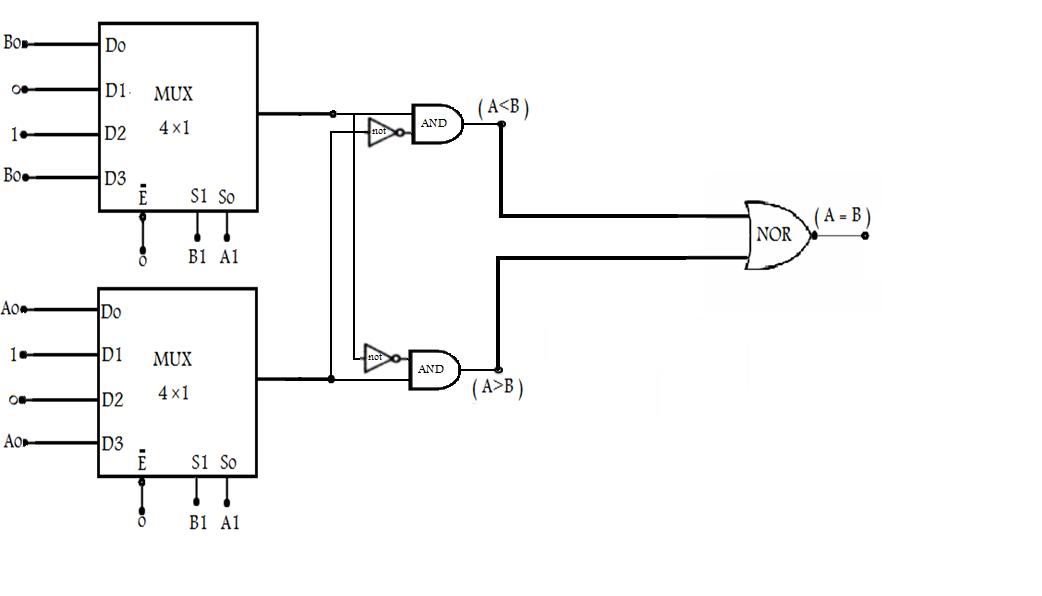
**Problem: Building Comparator Circuit:**

A 4-input, 3-output circuit that compares 2-bit unsigned numbers and

output a (1) on one of three output lines according to whether the first

number is greater than, equal to, or less than the other number. You can

only use two 4×1 multiplexers.(solution in fig.1)



**Fig(1)**