

Mechanical Engineering Department

**DIGITAL LABORATORY**

ENCS 211

**EXPERIMENT #5**

**Sequential Logic Circuits**

**Report**

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**Sec: two**

* **Abstract :**

In this experiment we were able to understand the differences between combinational and sequential circuits, and the use of memory including flip-flops and the operation of latches, but in concentrating in flip-flops, using these flip flop we were able to make counters and shift registers using “D”, “T”, and “JK” flip-flops each of them had different connection way finally we studied synchronous and asynchronous counters.

* **Objectives :**
* To understand the differences between combinational and sequential logic circuits; and the applications of various memory units.
* To study the operating principles and applications of various flip.
* To understand the operating principles of counters and how to construct counters with JK flip-flops.
* To study asynchronous and synchronous counters.
* **Apparatus :**

1. KL-22001 Basic Electricity Circuit Lab

2. KL-26006 sequence Logic Circuit Experiment Module (1)

3. KL-26007 sequence Logic Circuit Experiment Module (2)

4. Oscilloscope

* **Procedure and Data:**
* **Constructing master-slave JK flip-flop with RS flip-flop**



Figure 1: Showing the circuit of Master-Slave JK flip-flop using RS flip-flop.

By connecting the circuit in **Figure (1)**, we constructed the master –salve JK flip-flop, **CK1** should be connected to **Pulser switch**, **J** and **K** connected to inputs (**switches**), **F1**, **F2**, **F6**, and **F7** have been connected to logic indicators, after following the sequence in table below we got these results

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |
| CLK | **K** | **J** | **F1(S)** | **F2(R)** | **F6(Q)** | **F7(Ǭ(** | **→** | **F1(S)** | **F2(R) F6(Q)** | **F7(Ǭ)** |
| П | 0 | 0 | 0 | 0 | 0 | 1 |  | 0 | 0 0 | 1 |
| П | 0 | 1 | 0 | 0 | 0 | 1 |  | 1 | 0 1 | 0 |
| П | 1 | 0 | 1 | 0 | 1 | 0 |  | 0 | 0 0 | 1 |
| П | 1 | 1 | 0 | 0 | 0 | 1 |  | 1 | 0 1 | 0 |
| П | 1 | 1 | 1 | 0 | 1 | 0 |  | 0 | 0 0 | 1 |

* **Constructing Shift Register With “D” Flip-Flop**

After locating block “**a”** in 26006 module we connected the circuit, Clear (B) was connected to switch 0, A (I/P) connected to switch 1, CK connected to SWA and, the outputs **F1**, **F2**, **F3**, **F4** were connected to logic indicators.

By setting SW0 to “1” then to “0”, and SW1 to “1”, then applying 4 clock pulses to CK using SWA we got these data in the table below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| CLK | **F1** | **F2** | **F3** | **F4** |
| 1 | **1** | **0** | **0** | **0** |
| 2 | **1** | **1** | **0** | **0** |
| 3 | **1** | **1** | **1** | **0** |
| 4 | **1** | **1** | **1** | **1** |

* **Preset Left/Right Shift Register**

Looking at block “b” in 26006 module and connecting then inputs A, B, C, D to switches, and the outputs F1, F2, F3, F4 were connected to logic indicators , D1(Load) to SWA output, C1(CK) to SWB, B1(serial input) to SW7, and A1(Mode) to SW6

Then the sequence in the tables below was followed and we got these results

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | | |  | | | |
| INPUT | | | **OUTPUT** | | | |
| C1 | B1 | A1 | F1 | F2 | F3 | F4 |
| П | 1 | 0 | 1 | 0 | 0 | 0 |
| П | 1 | 0 | 1 | 1 | 0 | 0 |
| П | 1 | 0 | 1 | 1 | 1 | 0 |
| П | 1 | 0 | 1 | 1 | 1 | 1 |
| П | 1 | 0 | 1 | 1 | 1 | 1 |
| П | 0 | 0 | 0 | 1 | 1 | 1 |
| П | 0 | 0 | 0 | 0 | 1 | 1 |
| П | 0 | 0 | 0 | 0 | 0 | 1 |
| П | 0 | 0 | 0 | 0 | 0 | 0 |
| П | 0 | 0 | 0 | 0 | 0 | 0 |

Then by setting A1 and B1 to “1”, and the sequence in the next table was followed we got these results

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | | |  | | | |
| INPUT | | | **OUTPUT** | | | |
| C1 | D | C B A | F1 | F2 | F3 | F4 |
| П | 0 | 0 1 0 | 0 | 1 | 0 | 0 |
| П | 1 | 0 1 0 | 0 | 1 | 0 | 1 |
| П | 1 | 1 1 0 | 0 | 1 | 1 | 1 |
| П | 0 | 1 1 1 | 1 | 1 | 1 | 0 |
| П | 0 | 1 1 0 | 0 | 1 | 1 | 0 |

* **Constructing Divide-by-8 Counter With JK Flip-Flop**



The circuit in the previous page was connected, CK input was connected to pulser switch SW, Q1, Q2, and Q3 were connected to logic indicators, then pulses were applied and we get these results

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| CLK | **Q3**  **L5** | **Q2**  **L6** | **Q1**  **L7** |
| П | 1 | 0 | 0 |
| П | 1 | 0 | 1 |
| П | 1 | 1 | 0 |
| П | 1 | 1 | 1 |
| П | 0 | 0 | 0 |
| П | 0 | 0 | 1 |
| П | 0 | 1 | 0 |
| П | 0 | 1 | 1 |
| П | 1 | 0 | 0 |
| П | 1 | 0 | 1 |
| П | 1 | 1 | 0 |

* **Constructing Divide-by-8 counter with 7490**



After connecting the circuit above and connect J to SWA, and the outputs A, B, C, D to logic indicators, then by applying pulses and observation we got these results in the next page

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| CLK | **A**  **L5** | **B**  **L6** | **C**  **L7** | **D**  **L8** |
| П | 1 | 0 | 0 | 0 |
| П | 0 | 1 | 0 | 0 |
| П | 1 | 1 | 0 | 0 |
| П | 0 | 0 | 1 | 0 |
| П | 1 | 1 | 1 | 0 |
| П | 0 | 1 | 1 | 0 |
| П | 1 | 0 | 0 | 0 |
| П | 0 | 0 | 0 | 0 |
| П | 1 | 1 | 0 | 0 |
| П | 0 | 1 | 0 | 0 |

* **Constructing BCD Counter with 7490**



At first J input was connected to SWA, and the outputs A, B, C, D were connected to the inputs of Digital display D1, and the sequence was followed to get these results in the next page

|  |  |
| --- | --- |
|  |  |
| J | **D1** |
| П | 0 |
| П | 1 |
| П | 2 |
| П | 3 |
| П | 4 |
| П | 5 |
| П | 6 |
| П | 7 |
| П | 8 |
| П | 9 |

* **Conclusion :**

We noted that the characteristic of flip flop is applied in the table of present and next state. For T flip flop the equation is Q_{next} = T\overline{Q} + \overline{T}Q.

For JK Q_{next} = J\overline Q + \overline KQ . In [digital logic](http://en.wikipedia.org/wiki/Digital_logic) and [computing](http://en.wikipedia.org/wiki/Computing), a counter is a device which stores (and sometimes displays) the number of times a particular [event](http://en.wikipedia.org/wiki/Event_%28philosophy%29) or [process](http://en.wikipedia.org/wiki/Process_%28general%29) has occurred, often in relationship to a [clock signal](http://en.wikipedia.org/wiki/Clock_signal) & A flip-flop is usually controlled by one or two control [signals](http://en.wikipedia.org/wiki/Signals) and/or a gate or [clock signal](http://en.wikipedia.org/wiki/Clock_signal). The [output](http://en.wikipedia.org/wiki/Output) often includes the [complement](http://en.wikipedia.org/wiki/Complement) as well as the normal output. As flip-flops are implemented electronically, they require [power](http://en.wikipedia.org/wiki/Electric_power) and [ground](http://en.wikipedia.org/wiki/Ground_%28electricity%29) connections.