**Sequential Logic Circuits**

**OBJECTIVES**

-To understand the differences between combinational and sequential logic circuits; and the applications of various memory units.

-To study the operating principles and applications of various flip

-To understand the operating principles of counters and how to construct counters with JK flip-flops.

- To study asynchronous and synchronous counters.

**APPARATUS**

1. KL-22001 Basic Electricity Circuit Lab

2. KL-26006 sequence Logic Circuit Experiment Module (1)

3. KL-26007 sequence Logic Circuit Experiment Module (2)

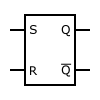
4. Oscilloscope

**THEORY**

n [digital circuits](http://en.wikipedia.org/wiki/Digital_circuit), a **flip-flop** is a term referring to an [electronic circuit](http://en.wikipedia.org/wiki/Electronic_circuit) (a [bistable](http://en.wikipedia.org/wiki/Bistable) [multivibrator](http://en.wikipedia.org/wiki/Multivibrator)) that has two stable states and thereby is capable of serving as one [bit](http://en.wikipedia.org/wiki/Bit) of [memory](http://en.wikipedia.org/wiki/Computer_storage). Today, the term *flip-flop* has come to mostly denote *non-transparent* (*clocked* or *edge-triggered*) devices, while the simpler *transparent* ones are often referred to as [latches](http://en.wikipedia.org/wiki/Latch_%28electronics%29); however, as this distinction is quite new, the two words are sometimes used interchangeably (see history).

A flip-flop is usually controlled by one or two control [signals](http://en.wikipedia.org/wiki/Signals) and/or a gate or [clock signal](http://en.wikipedia.org/wiki/Clock_signal). The [output](http://en.wikipedia.org/wiki/Output) often includes the [complement](http://en.wikipedia.org/wiki/Complement) as well as the normal output. As flip-flops are implemented electronically, they require [power](http://en.wikipedia.org/wiki/Electric_power) and [ground](http://en.wikipedia.org/wiki/Ground_%28electricity%29) connections.

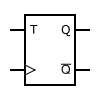
**Set-Reset flip-flops (SR flip-flops)**

[](http://en.wikipedia.org/wiki/Image:SR_Flip-flop.svg)

.The most fundamental latch is the simple *flip-flop* , where S and R stand for *set* and *reset* respectively. It can be constructed from a pair of cross-coupled [NOR](http://en.wikipedia.org/wiki/NOR_gate) (Not [OR](http://en.wikipedia.org/wiki/OR_gate)) [logic gates](http://en.wikipedia.org/wiki/Logic_gate). The stored bit is present on the output marked Q.

Normally, in storage mode, the S and R inputs are both [low](http://en.wikipedia.org/wiki/Bit#Representation), and [feedback](http://en.wikipedia.org/wiki/Feedback) maintains the Q and Q outputs in a constant state, with Q the complement of Q. If S (*Set*) is pulsed [high](http://en.wikipedia.org/wiki/Bit#Representation) while R is held low, then the Q output is forced high, and stays high even after S returns low; similarly, if R (*Reset*) is pulsed high while S is held low, then the Q output is forced low, and stays low even after R returns low.

**Toggle flip-flops (T flip-flops)**

[](http://en.wikipedia.org/wiki/Image:T-Type_Flip-flop.svg)

[http://en.wikipedia.org/skins-1.5/common/images/magnify-clip.png](http://en.wikipedia.org/wiki/Image:T-Type_Flip-flop.svg)

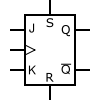
A circuit symbol for a T-type flip-flop, where > is the clock input, T is the toggle input and Q is the stored data output.

If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. This behavior is described by the characteristic [equation](http://en.wikipedia.org/wiki/Equation):

Q_{next} = T \oplus Q(or, without benefit of the [XOR](http://en.wikipedia.org/wiki/XOR_gate) operator, the equivalent: Q_{next} = T\overline{Q} + \overline{T}Q)

## JK flip-flop

The **JK** flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting J = K = 0 does NOT result in a D flip-flop, but rather, will hold the current state. To synthesize a D flip-flop, simply set K equal to the complement of J. The JK flip-flop is therefore a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop, or a T flip-flop. NOTE: The flip flop is positive edge triggered (Clock Pulse) as seen in the timing diagram.

[](http://en.wikipedia.org/wiki/Image:JK_Flip-flop.svg)

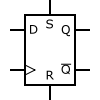
[http://en.wikipedia.org/skins-1.5/common/images/magnify-clip.png](http://en.wikipedia.org/wiki/Image:JK_Flip-flop.svg)

A circuit symbol for a JK flip-flop, where > is the clock input, J and K are data inputs, Q is the stored data output, and Q' is the inverse of Q.

The characteristic equation of the JK flip-flop is:

Q_{next} = J\overline Q + \overline KQ

**D flip-flop**

[](http://en.wikipedia.org/wiki/Image:D-Type_Flip-flop.svg)

[http://en.wikipedia.org/skins-1.5/common/images/magnify-clip.png](http://en.wikipedia.org/wiki/Image:D-Type_Flip-flop.svg)

D flip-flop symbol

The Q output always takes on the state of the D input at the moment of a rising clock edge. (or falling edge if the clock input is active low)[[6]](http://en.wikipedia.org/wiki/Flip-flop_%28electronics%29#cite_note-5) It is called the **D** flip-flop for this reason, since the output takes the value of the **D** input or *Data* input, and *Delays* it by one clock count. The D flip-flop can be interpreted as a primitive memory cell, [zero-order hold](http://en.wikipedia.org/wiki/Zero-order_hold), or [delay line](http://en.wikipedia.org/wiki/Delay_line).

# Counter

In [digital logic](http://en.wikipedia.org/wiki/Digital_logic) and [computing](http://en.wikipedia.org/wiki/Computing), a **counter** is a device which stores (and sometimes displays) the number of times a particular [event](http://en.wikipedia.org/wiki/Event_%28philosophy%29) or [process](http://en.wikipedia.org/wiki/Process_%28general%29) has occurred, often in relationship to a [clock signal](http://en.wikipedia.org/wiki/Clock_signal). In practice, there are two types of counters:

-up counters, which increase ([increment](http://en.wikipedia.org/wiki/Increment)) in value

-down counters, which decrease ([decrement](http://en.wikipedia.org/wiki/Decrement)) in value

**PROCEDURE**

**Flip-Flops**

**A. Constructing RS Flip-Flop with Basic Logic Gates**

Set the KL-26006 Module on the KL-22001 Basic electricity Circuit Lab, and

locate block c. Apply +5VDC and +12VDC from the Fixed Power on KL-22001

Lab to KL-26006 Module.then Connect inputs A3, A4 to Data Switches SW1 and SW2, respectively. Connect outputs F6 and F7 to logic Indicators L1, L2 & Turn the power off for a few seconds and turn it back on.

F6 & F7 are 0 1, after turn off they become 1 0.

3- the input sequences

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| state | A4 | A3 | F6 | F7 |
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 2 | 1 | 0 | 1 | 0 |
| 3 | 1 | 1 | 1 | 0 |

4-

|  |  |  |  |
| --- | --- | --- | --- |
| R | S | Q**n+1** | Q **n+1** |
| 0 | 0 | No change | unpredictable |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | unpredictable | No change |

Complete the connections by referring to the circuit in Fig 1.9 connect CK2 to +5V.& Connect inputs A1 and A5 to Data Switches SW1and SW2, respectively.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| state | A5 | A1 | F6 | F7 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 2 | 1 | 0 | 0 | 1 |
| 3 | 1 | 1 | 1 | 1 |

**B. Constructing D Flip-Flop with RS Flip-Flop.**

Complete the connections by referring to the D flip-flop circuit in Fig1.10. then Connect A1 to SW1, CK2 to the A output of Pulser Switch SWA and F6 to Logic Indicator L1.

& Follow the input sequences in Table 1.2. Observe and record the output

states.

|  |  |  |
| --- | --- | --- |
| clk | A1 | F6 |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| П | 0 | 0 |
| П | 1 | 1 |

**Constructing JK Flip-Flop with RS Flip-Flop**

Complete the connection by referring to the JK flip-flop circuit in Fig1.11 then Connect CK2 to the A output of Pulser Switch SWA, A1 to Data Switch SW1, and F6 to Logic Indicator L1& Follow the input sequences in Table 1.4. Observe and record output states.

|  |  |  |  |
| --- | --- | --- | --- |
| clk | A5 | A1 | F6 |
| П | 0 | 0 | 1 |
| П | 0 | 1 | 1 |
| П | 1 | 0 | 0 |
| П | 1 | 1 | 1 |

**D. constructing Master-Slave JK Flip-Flop with RS Flip-Flop**

Complete the connections by referring to the master-slave JK flip-flop circuit

in Fig 1.12. then Connect CK1 to the A output of Pulser Switch SWA, J and K to Data Switches SW0 and SW1. Connect F1,F2, F6, F7 to Logic Indicators L0, L1, L2, L3 Respectively& Follow the input sequences in the table 1.6 Observe and record the output states.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| clk | K | J | F1 | F2 | F6 | F7 | → | F1 | F2 F6 | F7 |
| П | 0 | 0 | 1 | 0 | 1 | 0 |  | 1 | 0 1 | 0 |
| П | 0 | 1 | 1 | 0 | 1 | 0 |  | 1 | 0 1 | 0 |
| П | 1 | 0 | 1 | 0 | 1 | 0 |  | 0 | 1 0 | 1 |
| П | 1 | 1 | 0 | 1 | 0 | 1 |  | 1 | 0 1 | 0 |
| П | 1 | 1 | 1 | 0 | 1 | 0 |  | 0 | 1 0 | 1 |

**E. Constructing Shift Register with D Flip-Flops**

Set the KL-26006 Module on the KL-22001 Basic Electricity Circuit Lab, and

locate block a. Apply +5VDC and +12VDC from the Fixed Power on KL-22001 lab to KL-26006 Module then Connect B(clear) to SW0; A(I/P) to SW1; CK to SWA output; F1,F2,F3,F4 to L1,L2,L3,L4 respectively then Set SW0 to "1" to clear D flip-flop, and then set to "0". Set SW1 to "1". Apply four clock pulses to CK using Pulser Switch SWA.

B=1 (preset) A=1(input)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| clk | F1 | F2 | F3 | F4 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |

Set SW0 to “1” to clear D flip-flops, and then set to “0”. Set SW1 to “1” and

return to “0” after one clock pulse in applied. Then apply three clock

pulses to CK using Pulser Switch SWA. Observe the output indications after

each pulse is applied

B=1 A=1 only in the first clk cycle then A=0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| clk | F1 | F2 | F3 | F4 |
| 1 | 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 0 | 1 |

**Preset Left/Right Shift Register**

Set the KL-26006 Module on the KL-22001 Basic Electricity Circuit Lab,

and locate block b. Apply +5VDC from the Fixed Power on KL-2201 Lab

to KL-26006 Module then Complete the following connections:

Inputs A,B,C,D to SW0, SW1, SW2, SW3

Outputs F1, F2, F3, F4 to L4, L3, L2, L1

D1 (LOAD) to SWA A output

C1 (CK) to SWB B output

B1 (Serial input) to SW7

A1 (MODE) to SW6

|  |  |
| --- | --- |
| INPUT | OUTPUT |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| C1 | B1 | A1 | F1 | F2 | F3 | F4 |
| П | 1 | 0 | 1 | 0 | 0 | 0 |
| П | 1 | 0 | 1 | 1 | 0 | 0 |
| П | 1 | 0 | 1 | 1 | 1 | 0 |
| П | 1 | 0 | 1 | 1 | 1 | 1 |
| П | 1 | 0 | 1 | 1 | 1 | 1 |
| П | 0 | 0 | 0 | 1 | 1 | 1 |
| П | 0 | 0 | 0 | 0 | 1 | 1 |
| П | 0 | 0 | 0 | 0 | 0 | 1 |
| П | 0 | 0 | 0 | 0 | 0 | 0 |
| П | 0 | 0 | 0 | 0 | 0 | 0 |

Set A1 and B1 to “1”. Follow the input sequences for D, C, B, A in Table1.9 Observe and record the outputs

|  |  |
| --- | --- |
| INPUT | OUTPUT |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| C1 | D | C B A | F1 | F2 | F3 | F4 |
| П | 0 | 0 1 0 | 1 | 0 | 0 | 0 |
| П | 1 | 0 1 0 | 1 | 1 | 0 | 0 |
| П | 1 | 1 1 0 | 1 | 1 | 1 | 0 |
| П | 0 | 1 1 1 | 1 | 1 | 1 | 1 |
| П | 0 | 1 1 0 | 1 | 1 | 1 | 1 |

**Counters**

**A-Construct Divide-by-8 Counter with JK Flip-Flops**

Set the KL-26007 Module on the KL-22001 Basic Electricity Circuit Lab, and

Locate block c. Complete the connections by referring to the wiring diagram

in Fig 1.15. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26007

Module then Connect CK input to the A output of Pulser Switch SW then Connect outputs Q1, Q2, and Q3 to Logic Indicators L5, L6, and L7, respectively. & Apply clock pulses to CK input using Pulser switch SWA. Observe and record the output Q1, Q2, and Q3 in Table 1.10

|  |  |  |  |
| --- | --- | --- | --- |
| CLK | Q3 | Q2 | Q1 |
| П | 1 | 1 | 1 |
| П | 0 | 0 | 0 |
| П | 0 | 0 | 1 |
| П | 0 | 1 | 0 |
| П | 0 | 1 | 1 |
| П | 1 | 0 | 0 |
| П | 1 | 0 | 1 |
| П | 1 | 1 | 0 |
| П | 1 | 1 | 1 |

**Constructing Synchronous Counter with JK Flip-Flops**

Set the KL-26007 Module on the KL-22001 basic Electricity Circuit Lab, and

locate block c. Complete the connections by referring to the wiring diagram

in Fig 1.16. Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26007

Module. Tthen Connect CK1 input to the A output of Pulser Switch SWA then Connect outputs Q2 and Q3 to Logic Indicators L6 and L7, respectively & Apply clock pulses to CK1 input using Pulser switch SWA. Observe and record

the outputs Q2 and Q3 in Table 1.11

|  |  |  |
| --- | --- | --- |
| CLK | Q3 | Q2 |
| П | 1 | 1 |
| П | 1 | 0 |
| П | 0 | 0 |
| П | 0 | 1 |
| П | 1 | 1 |
| П | 1 | 0 |
| П | 0 | 0 |

**C. Constructing Divide-by-8 Counter with 7490**

Set the KL-26007 Module on the KL-22001 Basic Electricity Circuit Lab, and

locate block b. Complete the connection by referring to the wiring diagram

in Fig 1.17 then Connect J input to the A output of Pulser Switch SWA then Connect output A, B, C, D to Logic Indicators L5, L6, L7, L8, respectively &Apply clock pulses to J input using Pulser switch SWA. Observe and record the

outputs A,B,C,D in Table 1.12

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| clk | A | B | C | D |
| П | 0 | 1 | 0 | 0 |
| П | 1 | 1 | 0 | 0 |
| П | 0 | 0 | 1 | 0 |
| П | 1 | 0 | 1 | 0 |
| П | 0 | 1 | 1 | 0 |
| П | 1 | 1 | 1 | 0 |
| П | 0 | 0 | 0 | 0 |
| П | 1 | 0 | 0 | 0 |
| П | 0 | 1 | 0 | 0 |
| П | 1 | 1 | 0 | 0 |

**D. Constructing BCD Counter with 7490**

Set the KL-26007 Module on the KL-22001 Basic Electricity Circuit Lab, and

locate block b. Complete the connections by referring to the wiring diagram

in Fig 1.18. Apply +5VDC from the Fixed Power on KL-26001 lab to KL-26007

Module then Connect J input to the A output of Pulser Switch SWA.then Connect outputs A,B,C,D to inputs A,B,C,D of Digital Display D1 respectively &Apply clock pulses to J input using Pulser switch SWA. Observe and record the Digital Display D1 in Table 1.13

|  |  |
| --- | --- |
| J | D1 |
| П | 4 |
| П | 5 |
| П | 6 |
| П | 7 |
| П | 8 |
| П | 9 |
| П | 0 |
| П | 1 |
| П | 2 |
| П | 3 |
| П | 4 |
| П | 5 |
| П | 6 |

**CONCLUSION:**

We note that the characteristic of flip flop is applied in the table of present and next state. For T flip flop the equation is Q_{next} = T\overline{Q} + \overline{T}Q.

For JK Q_{next} = J\overline Q + \overline KQ . In [digital logic](http://en.wikipedia.org/wiki/Digital_logic) and [computing](http://en.wikipedia.org/wiki/Computing), a counter is a device which stores (and sometimes displays) the number of times a particular [event](http://en.wikipedia.org/wiki/Event_%28philosophy%29) or [process](http://en.wikipedia.org/wiki/Process_%28general%29) has occurred, often in relationship to a [clock signal](http://en.wikipedia.org/wiki/Clock_signal) & A flip-flop is usually controlled by one or two control [signals](http://en.wikipedia.org/wiki/Signals) and/or a gate or [clock signal](http://en.wikipedia.org/wiki/Clock_signal). The [output](http://en.wikipedia.org/wiki/Output) often includes the [complement](http://en.wikipedia.org/wiki/Complement) as well as the normal output. As flip-flops are implemented electronically, they require [power](http://en.wikipedia.org/wiki/Electric_power) and [ground](http://en.wikipedia.org/wiki/Ground_%28electricity%29) connections .