

**Faculty of Engineering & Technology**

**Electrical & Computer Engineering Department**

**DIGITAL ELECTRONICS AND COMPUTER**

**ORGANIZATION LABORATORY - ENCS2110**

**Report #1**

**Experiment #2&3**

**Comparators, Adders and Subtractors,**

**Encoders, Decoders, Multiplexer and Demultiplexer**

**Prepared by: ID:**

Ro’a Nafi 1201959

**Partners:** Manar Shawahni 1201086

Leelyan Karajah1201191

**Instructor**: Dr. Ahmad Alyan  
**Assistant**: Mahmoud Hussain

**Section:** 13

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# Abstract

our first experiment aims to understand the operating principle of digital comparators and construct it with basic gates. In addition, implement a half-adder, full-adders, 4-bit-adders, half-subtractor and full- subtractor.

Second experiment aims to understand the operating principle of the encoder, decoder, multiplexer and demultiplexer and construct each one of them using the basic gates.

Contents

[Abstract 2](#_Toc100527115)

[List of figures 5](#_Toc100527116)

[List of tables 6](#_Toc100527117)

[Theory 12](#_Toc100527118)

[1- comparator circuit 12](#_Toc100527119)

[a -1bit Comparator circuit 12](#_Toc100527120)

[b -4bit Comparator circuit 13](#_Toc100527121)

[2-Half adder 14](#_Toc100527122)

[3-Full Adder 15](#_Toc100527123)

[4- Half subtractor: 15](#_Toc100527124)

[5-Full subtractor 16](#_Toc100527125)

[6- Decoder 17](#_Toc100527126)

[2 to 4 Decoder 17](#_Toc100527127)

[7-Encoder 18](#_Toc100527128)

[4 to 2 Decoder 18](#_Toc100527129)

[8-Multiplexer 19](#_Toc100527130)

[4x1 Multiplexer 19](#_Toc100527131)

[Demultiplexer 20](#_Toc100527132)

[1X4 Demultiplexer 20](#_Toc100527133)

[**Demultiplexer** 20](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527134)

[Procedure 21](#_Toc100527135)

[1- comparator circuit 21](#_Toc100527136)

[1- comparator circuit with basic logic gates 21](#_Toc100527137)

[2- comparator circuit with TTL IC 21](#_Toc100527138)

[2- Half and Full adder circuit 22](#_Toc100527139)

[1- Half and Full adder circuit with basic logic gates 22](#_Toc100527140)

[2- 4-bit full adder 23](#_Toc100527141)

[3- BCD adder 24](#_Toc100527142)

[3- Half and full subtractors 25](#_Toc100527143)

[1- Half-/Full Subtractors with basic logic Gates. 25](#_Toc100527144)

[2- 4-Bit Full-Subtractor with IC 26](#_Toc100527145)

[4- 4-to-2 Encoder with Basic Gates 27](#_Toc100527146)

[5- 9-to-4-Line Encoder with TTL IC 28](#_Toc100527147)

[6- 2-to-4 Line Decoder with Basic Gates 28](#_Toc100527148)

[7- 4-to-10 Line Decoder with TTL IC 29](#_Toc100527149)

[8- 2-to-1-Line Multiplexer with basic Gates 29](#_Toc100527150)

[9-8-to-1 Line Multiplexer with IC 30](#_Toc100527151)

[10- 1-to-2 Line Demultiplexer with Basic Logic Gates 30](#_Toc100527152)

[11- 1-to-8-Line Demultiplexer with CMOS IC 31](#_Toc100527153)

[Conclusion 32](#_Toc100527154)

[References 33](#_Toc100527155)

# List of figures

[Figure 1: **comparator circuit – circuit symbol** 12](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527286)

[Figure 2: **comparator circuit – circuit diagram** 12](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527287)

[Figure 3 : 4-bit comparator circuit – circuit symbol 13](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527288)

[Figure 4: **4-bit comparator circuit – circuit diagram** 14](#_Toc100527289)

[Figure 5: Half adder circuit 14](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527290)

[Figure 6:Full adder circuit 15](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527291)

[Figure 7: Half subtractor circuit 15](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527292)

[Figure 8: Full subtractor circuit 16](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527293)

[Figure 9:Decoder circuit- circuit symbol Figure 10 : Decoder circuit 17](#_Toc100527294)

[Figure 11: Encoder circuit 18](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527295)

[Figure 12: Encoder circuit symbol 18](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527296)

[Figure13 18](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527297)

[Figure 14:Multiplexer circuit 19](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527298)

[Figure 15: Multiplexer circuit symbol 19](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527299)

[Figure 16:Demultiplexer circuit symbol 20](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527300)

[Figure 17:Demultiplexer circuit 20](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527301)

[Figure 18:Wiring diagram (IT-3002) 21](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527302)

[Figure 19:4-bit Comparator IC (IT-3002) 21](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527303)

[Figure 20: Wiring diagram (IT-3003 Half-Adder block) 22](#_Toc100527304)

[Figure 21: Wiring diagram (IT-3003 Full-Adder block) 23](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527305)

[Figure 22 : Wiring diagram (IT-3003 4bit Full-Adder block) 23](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527306)

[Figure 23 : 5 Wiring Diagram (IT-3003 BCD Adder) 24](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527307)

[Figure 24: Wiring diagram (Half-subtractor) 25](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527308)

[Figure 25:Wiring Diagram for full subtractor (IT-3003 4-bit Full-Adder block) 26](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527309)

[Figure 26: 3 wiring diagram of 4-to-2 line Encoder 27](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527310)

[Figure 27: 2-to-4 decoder 28](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527311)

[Figure 28 : 2-to-1 Multiplexer 29](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527312)

[Figure 29 : Demultiplexer 30](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527313)

# List of tables

[Table 1: **1-bit comparator Truth table** 12](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527181)

[Table 2 – half adder truth table 14](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527182)

[Table 3- full adder truth table 15](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527183)

[Table 4 : Half subtractor truth table 15](#_Toc100527184)

[Table 5: full-subtractor truth table 16](#_Toc100527185)

[Table 6:decoder truth table 17](#_Toc100527186)

[Table 7: Decoder truth table 18](#_Toc100527187)

[Table 8: Multiplexer truth table 19](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527188)

[Table 9:Demultiplexer truth table 20](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527189)

[Table 10: - comparator truth table 21](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527190)

[Table 11: 4-bit Comparator truth table 22](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527191)

[Table 12 : Half adder truth table 23](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527192)

[Table 13: 4bit full adder truth table 24](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527193)

[Table 14:BCD Adder truth table 25](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527194)

[Table 15: half subtractor truth table 26](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527195)

[Table 16 : 4-Bit Full-Subtractor truth table 26](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527196)

[Table 17: 4-to-2 line Encoder truth table 27](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527197)

[Table 18: 9-to-4 line Encoder truth table 28](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527198)

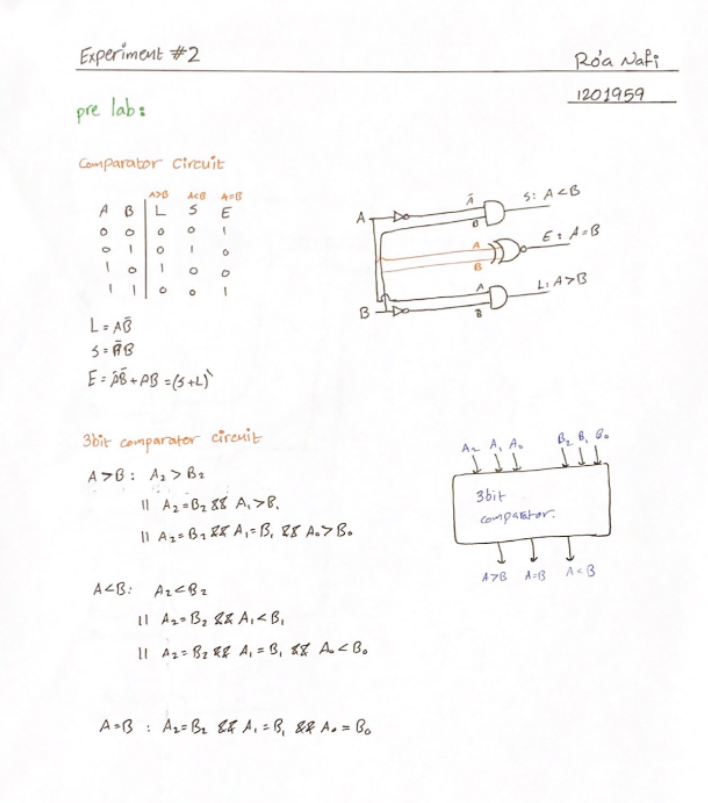
[Table 19: 2-to-4 decoder truth table 28](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527199)

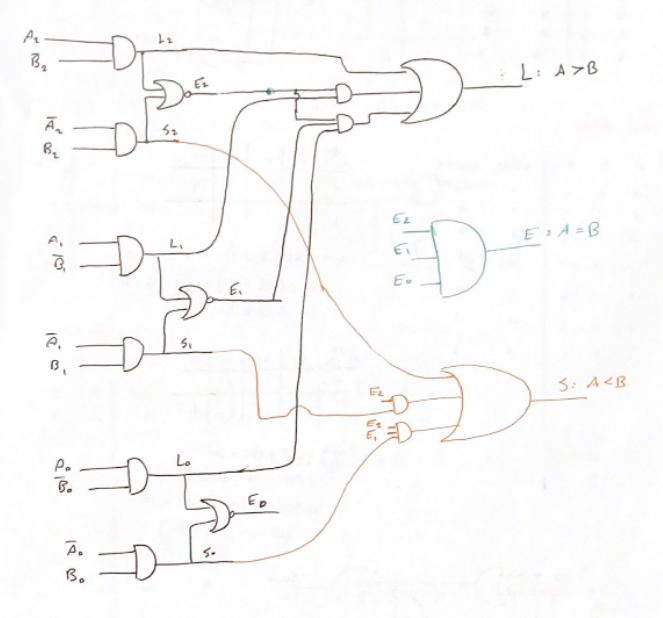
[Table 20 : 4-to-10 Line Decoder truth table 29](#_Toc100527200)

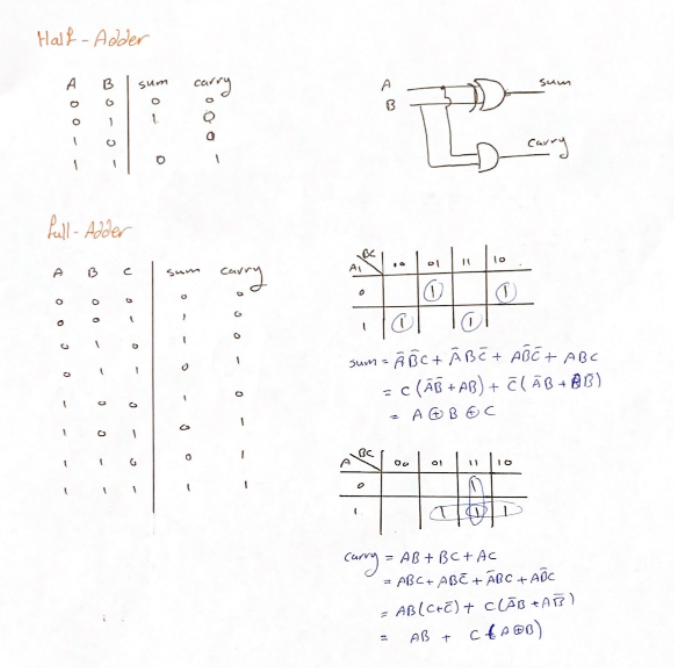
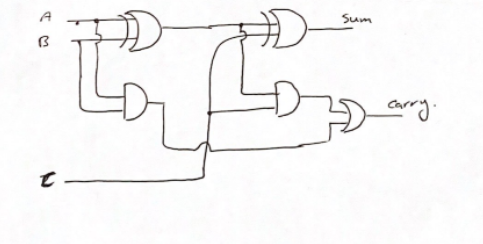
[Table 21:: 2-to-1 Multiplexer truth table 29](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527201)

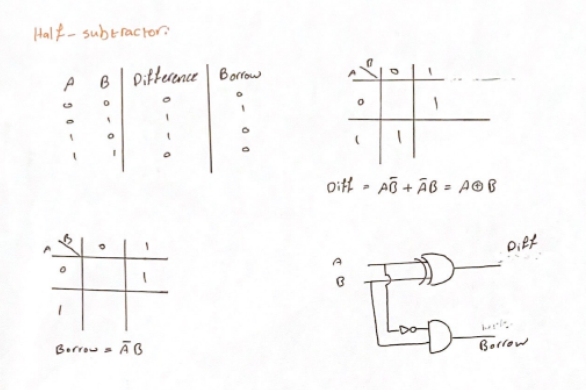
[Table 22:8-to-1 Line Multiplexer truth table 30](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527202)

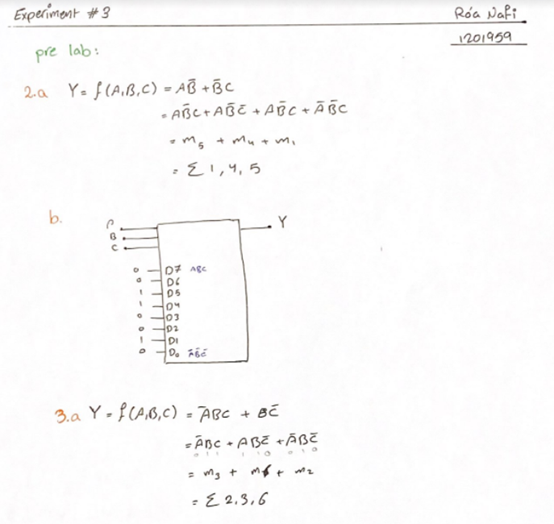
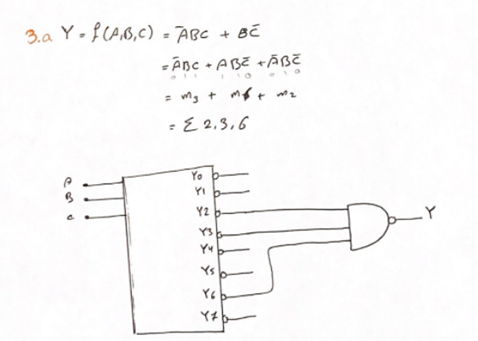
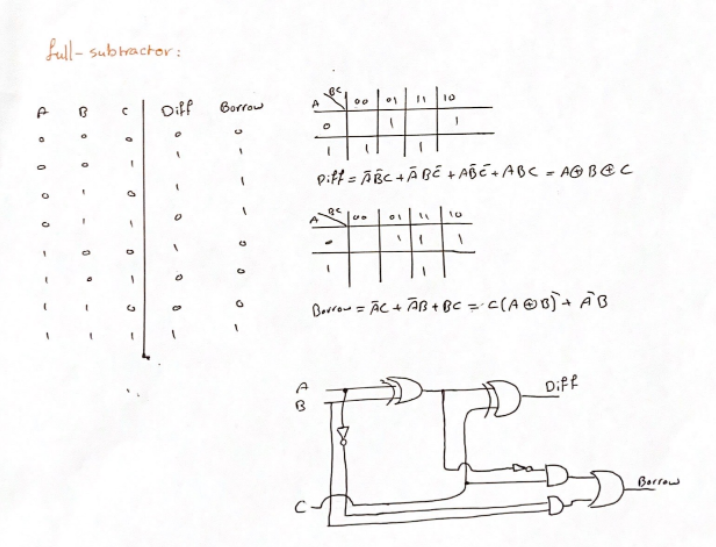
[Table 23: Demultiplexer truth table 31](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/Comparators%5eJ%20Adders%20and%20Subtractors.docx#_Toc100527203)







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# Theory

# 1- comparator circuit

A Comparator is a [combinational circuit](https://technobyte.org/sequential-combinational-logic-circuits-types/) that gives output in terms of A>B, A<B, and A=B. A digital comparator’s purpose is to compare numbers (At least two number are required) and represent their relationship with each other.

A=B

N-bit Comparator

A>B

A<B

A

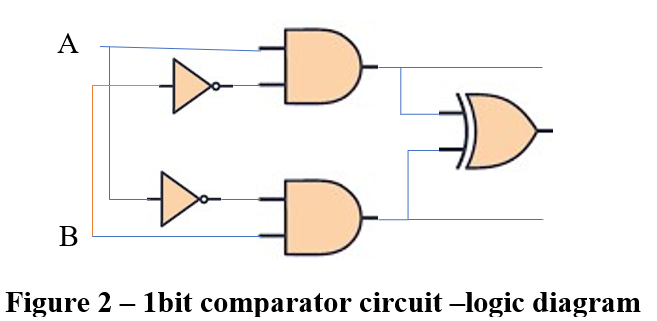
B

Figure : **comparator circuit – circuit symbol**

## a -1bit Comparator circuit

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | A>B | A=B | A<B |
| 0 | 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | 0 | |

Table : **1-bit comparator Truth table**

Boolean functions using k-map:

A>B

A > B equation = A.B’

A=B

A = B equation = A’B’ + AB

A<B

= A.B’ xor A’B

A < B equation = A’B

Figure : **comparator circuit – circuit diagram**

## b -4bit Comparator circuit

A[3:0]

4-bit Comparator

A>B

A=B

A<B

B[3:0]

Figure : 4-bit comparator circuit – circuit symbol

**A = B:**

this output is true:

A0 = B0, A1 = B1, A2 = B2, A3 = B3

**A > B:**

this output is true:

1. When A3 > B3

2. When A3 = B3 AND A2 > B2

3. When A3 = B3 AND A3 = B3 AND A2 > B2

4. When A3 = B3 AND A3 = B3 AND A2 = B2 AND A1 > B1

5. When A3 = B3 AND A3 = B3 AND A2 = B2 AND A1 = B1 AND A0 > B0

**A > B:**

this output is true:

1. When A3 < B3

2. When A3 = B3 AND A2 < B2

3. When A3 = B3 AND A3 = B3 AND A2 < B2

4. When A3 = B3 AND A3 = B3 AND A2 = B2 AND A1 < B1

5. When A3 = B3 AND A3 = B3 AND A2 = B2 AND A1 = B1 AND A0 < B0

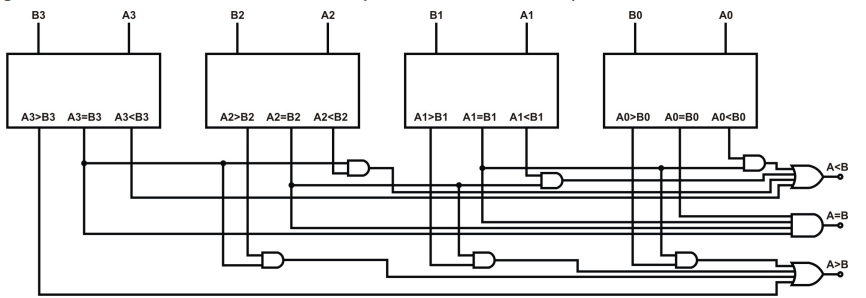


Figure : **4-bit comparator circuit – circuit diagram**

## 2-Half adder

[combinational circuit](https://technobyte.org/sequential-combinational-logic-circuits-types/) that used to add two bits.

|  |  |  |  |
| --- | --- | --- | --- |
| input | | output | |
| A | B | sum | carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table – half adder truth table



A

sum

Boolean functions Using k-map:

B

Sum = A xor B

carry

Carry = A.B

Figure 5: Half adder circuit

## 3-Full Adder

[combinational circuit](https://technobyte.org/sequential-combinational-logic-circuits-types/) that used to add three bits.

Figure 6:Full adder circuit

carry

sum m

Boolean functions Using k-map:

Sum = A xor B xor C

Carry = A.B + C.( A xor B)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| input | | | Output | |
| A | B | C | sum | carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 3- full adder truth table

## 4- Half subtractor:

|  |  |  |  |
| --- | --- | --- | --- |
| input | | output | |
| A | B | Difference | Borrow |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Boolean functions Using k-map:

Difference= A xor B

Borrow= A’.B

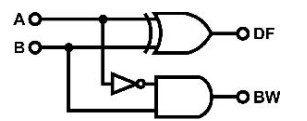


Figure : Half subtractor circuit

Table : Half subtractor truth table

7

## 5-Full subtractor

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| input | | | Output | |
| A | B | C | Difference | Borrow |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Boolean functions Using k-map:

Difference= A xor B xor C

Borrow= c.( A xor B)’ + A’B

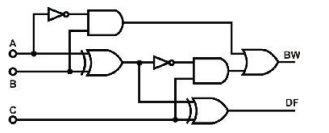


Figure : Full subtractor circuit

8

Table 5: full-subtractor truth table

## 6- Decoder

 combinational circuit has takes n inputs and maximum 2n outputs, one of these outputs will be active High.

### 2 to 4 Decoder

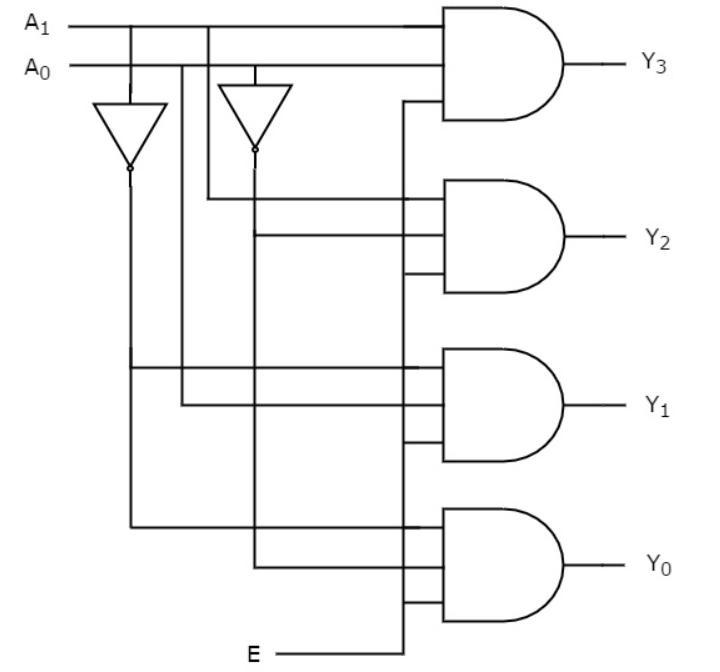
Boolean functions using K-map:

D0 = A’. B’

D1 = A’. B

D2 = A. B’

D3 = A. B

 Table 6:decoder truth table

D0

D1

D2

B

D3

A

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| input | | | Output | | | |
| E | A0 | A1 | D0 | D1 | D3 | D4 |
| 0 | X | X | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

A

2X4

Decoder

E

B

D2

D3

D1

D0

Figure 9:Decoder circuit- circuit symbol Figure : Decoder circuit

## 7-Encoder

combinational circuits that it has 2n inputs, and n outputs ,it performs the reverse operation of an decoder

### 4 to 2 Decoder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| input | | | | output | |
| D3 | D2 | D1 | D0 | A | B |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |

Boolean functions using K-map:

A=D3+D2

B=D3+D1

Table : Decoder truth table



D3

A

D0

A



Figure : Encoder circuit

Figure : Encoder circuit symbol

D2

Figure13

B

D3

D2

D1

B

4X2

Encoder

D1

## 8-Multiplexer

combinational circuit that has maximum of 2n data inputs, ‘n’ selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines.

### 4x1 Multiplexer

|  |  |  |
| --- | --- | --- |
| selection | | output |
| S1 | S0 | F |
| 0 | 0 | I0 |
| 0 | 1 | I1 |
| 1 | 0 | I2 |
| 1 | 1 | I3 |

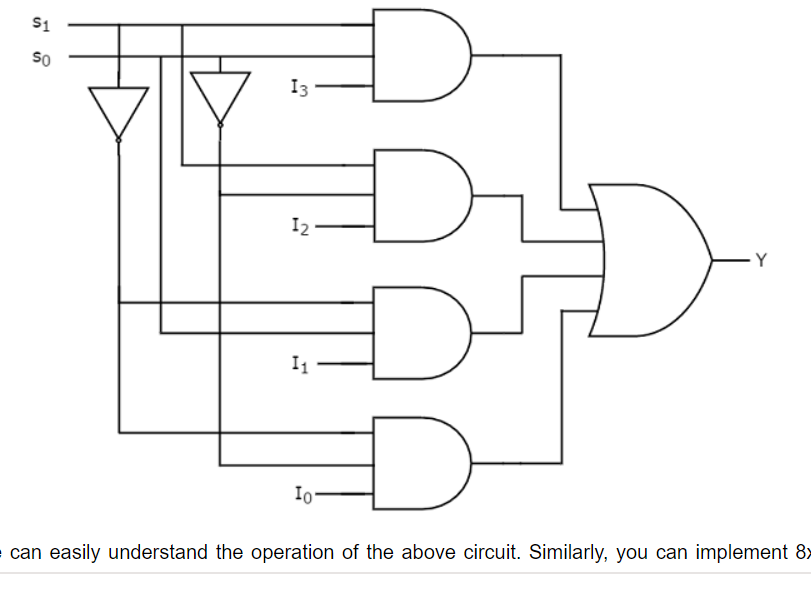


Figure :Multiplexer circuit

Figure : Multiplexer circuit symbol

F

Table : Multiplexer truth table

Boolean functions using K-map:

F= S1’S0’I0 + S1’S0I1 + S1S0’I2 + S1S0I3

4X1

Multiplexer

S0

S1

F

I3

I2

I1

I0

## Demultiplexer

combinational circuit that performs the reverse operation of Multiplexer. It has single input, ‘n’ selection lines and maximum of 2n outputs. The input will be connected to one of these outputs based on the values of selection lines.

### 1X4 Demultiplexer

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| selection | | output | | | |
| S1 | S0 | I0 | I1 | I2 | I3 |
| 0 | 0 | F | 0 | 0 | 0 |
| 0 | 1 | 0 | F | 0 | 0 |
| 1 | 0 | 0 | 0 | F | 0 |
| 1 | 1 | 0 | 0 | 0 | F |

I0

F

I1

1x4

## **Demultiplexer**

I2

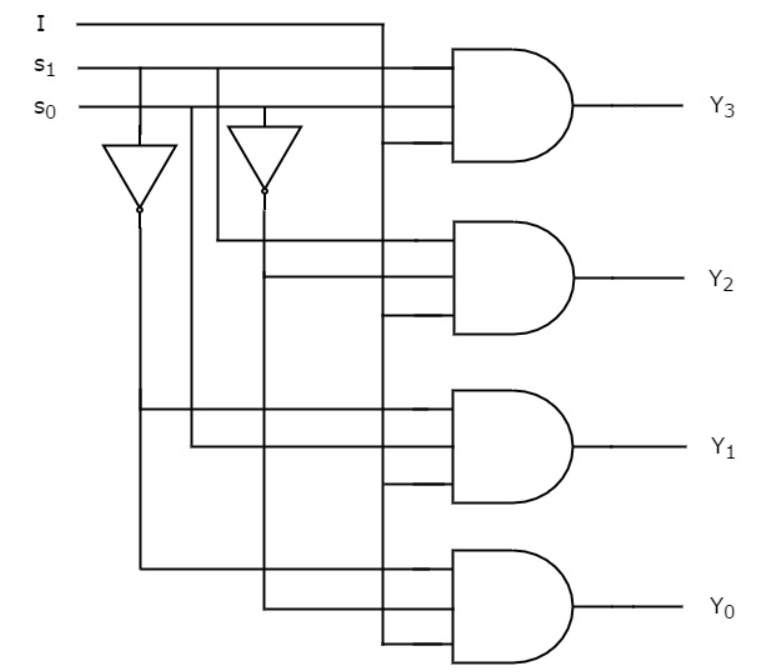


Table :Demultiplexer truth table

Boolean functions using K-map:

I3=S1S0F

I2=S1S0′ F

I1=S1′S0 F

I0=S1′S0′ F

Figure :Demultiplexer circuit symbol

I1

I2

I0

I3

S0

S1

F

I3

S1

S0

Figure :Demultiplexer circuit

# Procedure

## 1- comparator circuit

### 1- comparator circuit with basic logic gates

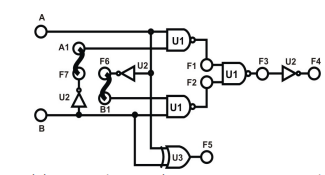
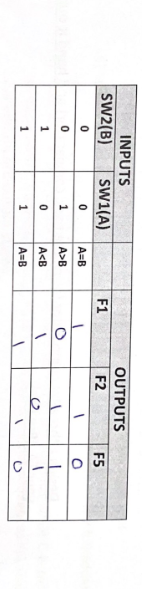


Figure :Wiring diagram (IT-3002)

Table : - comparator truth table

This result are exactly the opposite with theory ,since we used NAND and XOR gates instead of NOT, AND & NOR.

### 2- comparator circuit with TTL IC

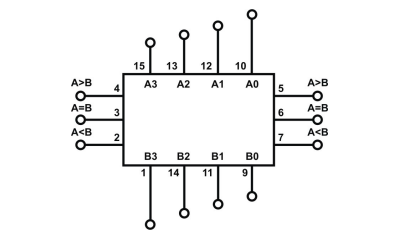


Figure :4-bit Comparator IC (IT-3002)

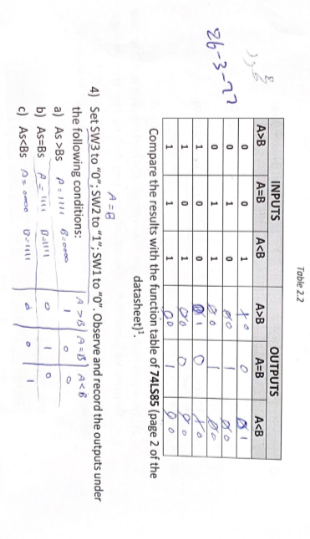


Table : 4-bit Comparator truth table

## 2- Half and Full adder circuit

### 1- Half and Full adder circuit with basic logic gates

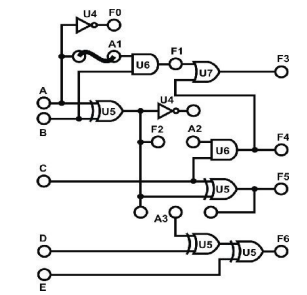


Figure : Wiring diagram (IT-3003 Half-Adder block)

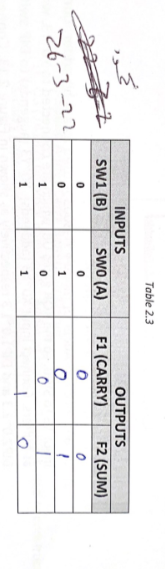


Table : Half adder truth table

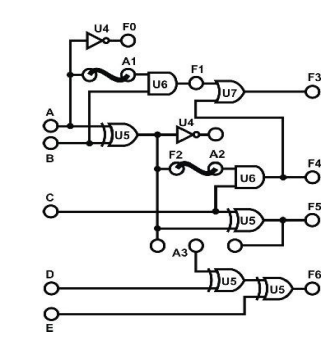


Figure : Wiring diagram (IT-3003 Full-Adder block)

### 2- 4-bit full adder

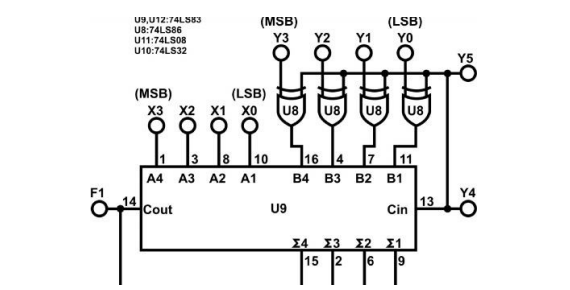


Figure : Wiring diagram (IT-3003 4bit Full-Adder block)

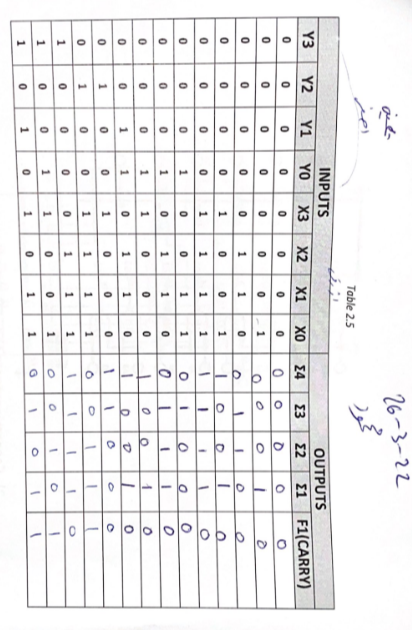
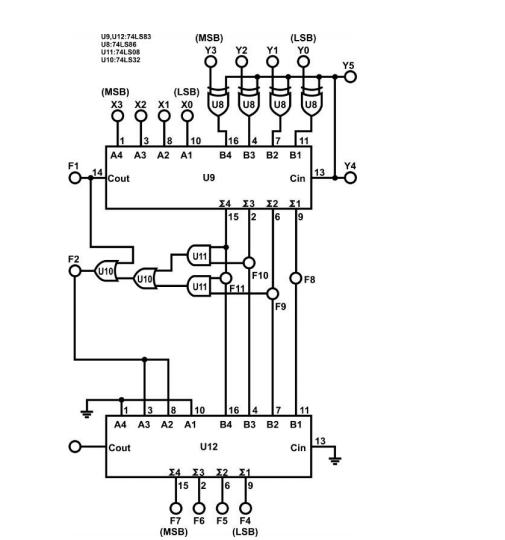


Table : 4bit full adder truth table



### 3- BCD adder

Figure : 5 Wiring Diagram (IT-3003 BCD Adder)

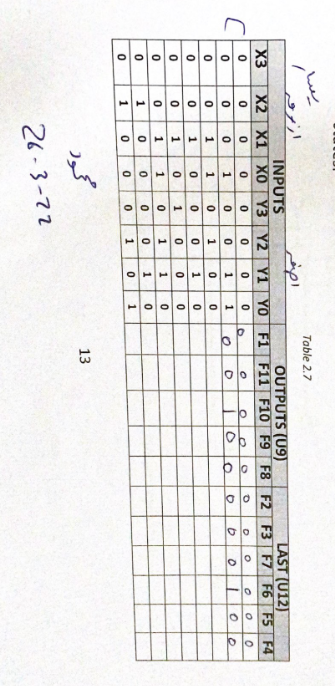
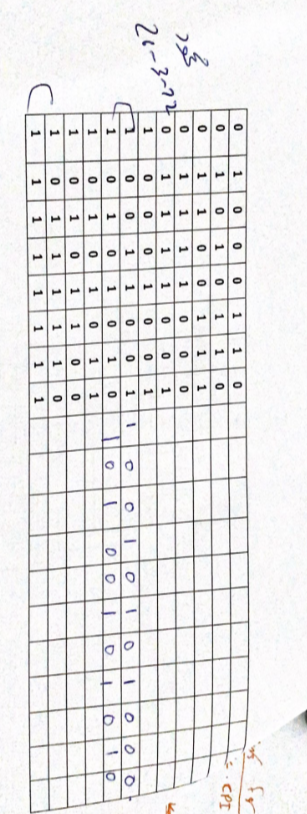


Table :BCD Adder truth table

## 3- Half and full subtractors

### 1- Half-/Full Subtractors with basic logic Gates.

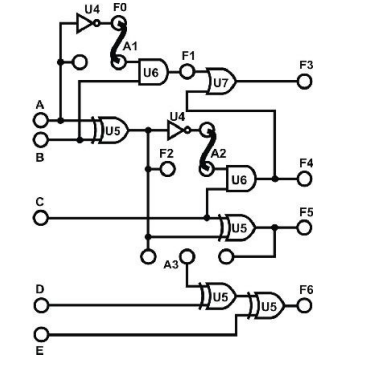
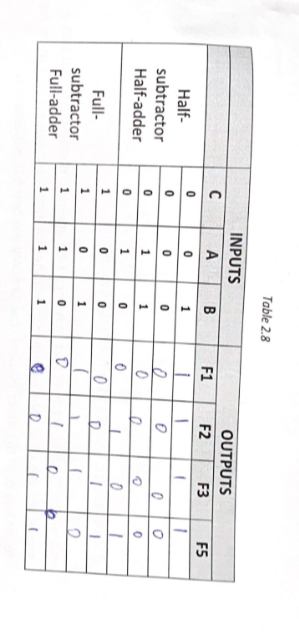


Figure : Wiring diagram (Half-subtractor)



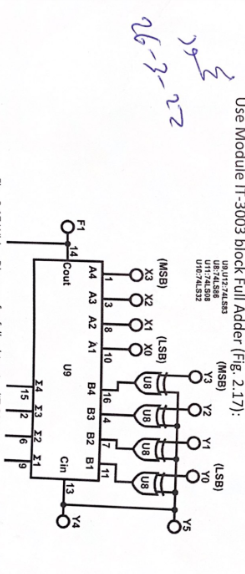


Table : half subtractor truth table

### 2- 4-Bit Full-Subtractor with IC

Figure :Wiring Diagram for full subtractor (IT-3003 4-bit Full-Adder block)

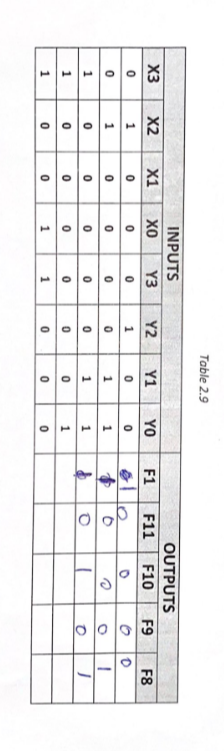
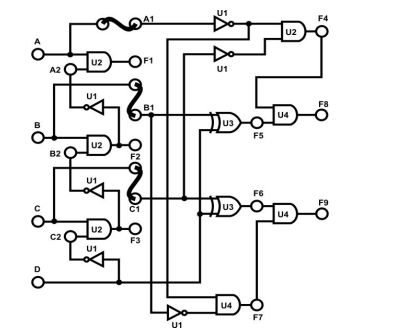


Table : 4-Bit Full-Subtractor truth table

## 4- 4-to-2 Encoder with Basic Gates



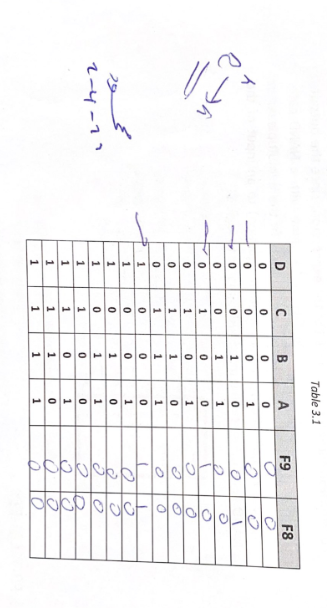
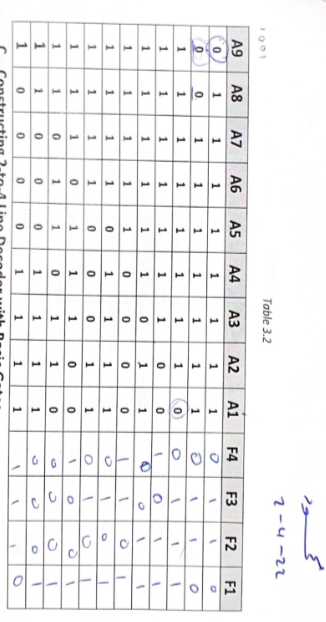


Figure : 3 wiring diagram of 4-to-2 line Encoder

Table : 4-to-2 line Encoder truth table



## 5- 9-to-4-Line Encoder with TTL IC

Table : 9-to-4 line Encoder truth table

## 6- 2-to-4 Line Decoder with Basic Gates

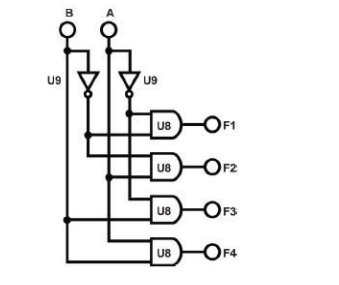
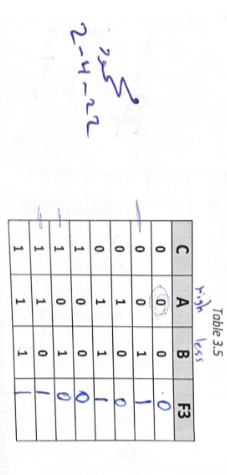


Table : 2-to-4 decoder truth table

Figure : 2-to-4 decoder

## 7- 4-to-10 Line Decoder with TTL IC

 Table : 4-to-10 Line Decoder truth table

## 8- 2-to-1-Line Multiplexer with basic Gates

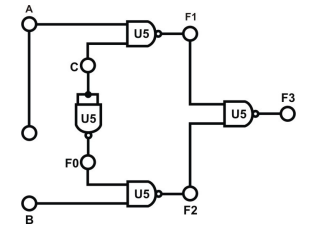


Table :: 2-to-1 Multiplexer truth table

Figure : 2-to-1 Multiplexer

The above table represents an active-high input-output multiplexer with C as the selection bit.

## 9-8-to-1 Line Multiplexer with IC

Table :8-to-1 Line Multiplexer truth table

 the output based on the inputs

## 10- 1-to-2 Line Demultiplexer with Basic Logic Gates



Figure : Demultiplexer

## 11- 1-to-8-Line Demultiplexer with CMOS IC

Table : Demultiplexer truth table

D is an active-low enable, when it was 1 it disables the demultiplexer, and while it's 0 it enables the demultiplexer and allows it to work properly.

# Conclusion

The experiment helped with understanding more about comparators and adders and subtractors decoders, encoders, multiplexers and demultiplexers.

All results were similar to the theoretical part for all of the circuits that have been constructed, no connection problems occurred while implementing the experiment.

# References

1- <https://www.tutorialspoint.com/index.htm>

2 lab manual