

**Faculty of Engineering & Technology**

**Electrical & Computer Engineering Department**

**DIGITAL ELECTRONICS AND COMPUTER**

**ORGANIZATION LABORATORY - ENCS2110**

**Report #2**

**Experiment #5**

**SEQUENTIAL LOGIC CIRCUITS**

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# Abstract

This experiment aims to understand the differences between combinational and sequential Logic circuits. In addition, to understand the operating principles of counters. study the operating principles and applications of various flip-flops, synchronous counters and asynchronous counters, how to construct counters with JK flip-flops.

Contents

[Abstract 2](#_Toc102175007)

[List of figures 4](#_Toc102175008)

[List of tables 5](#_Toc102175009)

[Pre lap 6](#_Toc102175010)

[7](#_Toc102175011)

[8](#_Toc102175012)

[9](#_Toc102175013)

[Theory 10](#_Toc102175014)

[1- Sequential Circuits 10](#_Toc102175015)

[2-Latches 10](#_Toc102175016)

[2.1- The SR (Set-Reset) Latch 10](#_Toc102175017)

[2.2-The D Latch 12](#_Toc102175018)

[3- Flip-Flops 12](#_Toc102175019)

[3.1-D Flip-Flop 12](#_Toc102175020)

[3.2- JK Flip-Flop 13](#_Toc102175021)

[3.3-T Flip-Flop 13](#_Toc102175022)

[4- Registers 13](#_Toc102175023)

[5- Counters 14](#_Toc102175024)

[PROCEDURE 15](#_Toc102175025)

[1-Latches and Flip flops 15](#_Toc102175026)

[1.1-Constructing RS latch with Basic Logic Gates 15](#_Toc102175027)

[1.2- Constructing RS latch with control input 15](#_Toc102175028)

[1.3-Constructing D latch with RS latch 16](#_Toc102175029)

[1.4- Constructing JK latch with RS latch 16](#_Toc102175030)

[2-Constructing JK Flip-flop with master- slave RS latches 17](#_Toc102175031)

[3- Registers 18](#_Toc102175032)

[3.1- Constructing Shift Register with D Flip-Flops 18](#_Toc102175033)

[3.2- 4-Bit Shift Register with serial and parallel load 19](#_Toc102175034)

[4-Counters 20](#_Toc102175035)

[4.1- 2-bit Synchronous Counter 20](#_Toc102175036)

[4-2: 3-bit (divide-by-eight) Ripple Counter 21](#_Toc102175037)

[4.3- BCD Counter 22](#_Toc102175038)

[Task 2: 23](#_Toc102175039)

[Task3: 23](#_Toc102175040)

[Conclusion 24](#_Toc102175041)

[DISCUSSION 24](#_Toc102175042)

[References: 26](#_Toc102175043)

# List of figures

[Table 2:SR latch with NAND gates Figure 1:SR latch with NAND gates 11](#_Toc102175076)

[Table 3:SR latch with NOR gates Figure 2:SR latch with NOR gates 12](#_Toc102175077)

[Table 6: D latch Figure 3:D latch 13](#_Toc102175078)

[Figure 4:negative edge flip flop 13](#_Toc102175079)

[Figure 5:D latch 13](#_Toc102175080)

[Table 7:JK Flip-Flop Figure 6:JK Flip-Flop 14](#_Toc102175081)

[Table 8:T flip flop Figure 7:T Flip-Flop 14](#_Toc102175082)

[Figure 8:: 4-bit Register 14](#_Toc102175083)

[Figure 9:3-bit ripple counters Figure 10:3-bit synchronous counters 15](#_Toc102175084)

[Figure 11:RS latch 16](#_Toc102175085)

[Figure 12:RC latch with control 16](#_Toc102175086)

[Figure 13:D latch 17](#_Toc102175087)

[Figure 14:JK latch with RS latch 17](#_Toc102175088)

[Figure 15:JK flip flop 18](#_Toc102175089)

[Figure 16:shift register with serial and parallel load 20](#_Toc102175090)

[Figure 17: 3-bit Ripple Counter 22](#_Toc102175091)

[Figure 18:3-bit Synchronous Counter. 24](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/EXP5.docx#_Toc102175092)

[Figure 19:- 0-to-5 counter 24](#_Toc102175093)

[Figure 20::- 0-to-4 counter 25](#_Toc102175094)

# List of tables

[Table 1:Sequential Circuits 11](#_Toc102175108)

[Table 2:SR latch with NAND gates Figure 1:SR latch with NAND gates 11](#_Toc102175109)

[Table 3:SR latch with NOR gates Figure 2:SR latch with NOR gates 12](#_Toc102175110)

[Table 4:RS latch with control input Table 5:RS latch with control input 12](#_Toc102175111)

[Table 6: D latch Figure 3:D latch 13](#_Toc102175112)

[Table 7:JK Flip-Flop Figure 6:JK Flip-Flop 14](#_Toc102175113)

[Table 8:T flip flop Figure 7:T Flip-Flop 14](#_Toc102175114)

[Table 9:RC latch 16](#_Toc102175115)

[Table 10:RC latch with control 16](#_Toc102175116)

[Table 11:D latch 17](#_Toc102175117)

[Table 12: JK latch with RS latch 17](#_Toc102175118)

[Table 13:JK flip flop 18](#_Toc102175119)

[Table 14:4-Bit Shift Register with serial and parallel load 20](#_Toc102175120)

[Table 15:4-Bit parallel load: 21](#_Toc102175121)

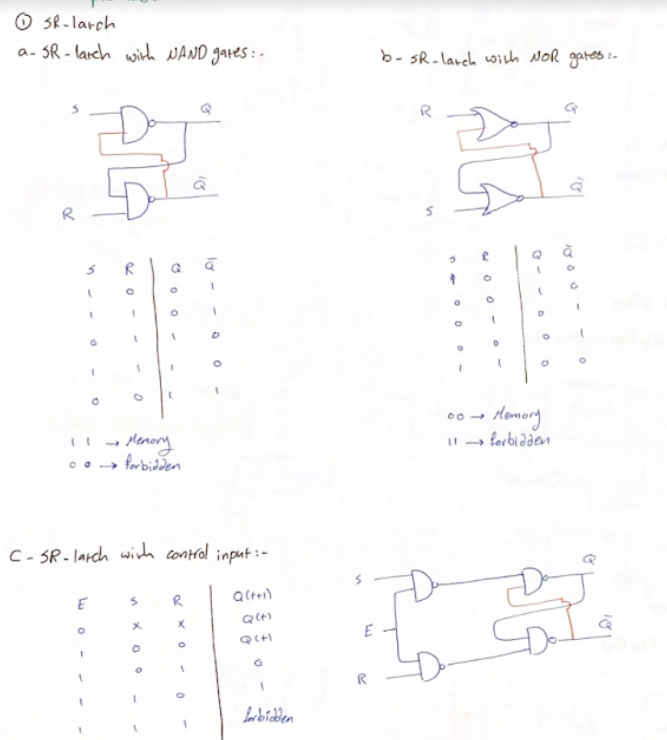
[Table 16:: 2-bit Synchronous Counter 21](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/EXP5.docx#_Toc102175122)

[Table 17:2-bit Synchronous Counter 21](https://d.docs.live.net/3d27aba67ca6cbda/Desktop/lab-digital/EXP5.docx#_Toc102175123)

[Table 18: 3-bit Ripple Counter 22](#_Toc102175124)

[Table 19:BCD counter 23](#_Toc102175125)

# Pre lap



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# Theory

## 1- Sequential Circuits

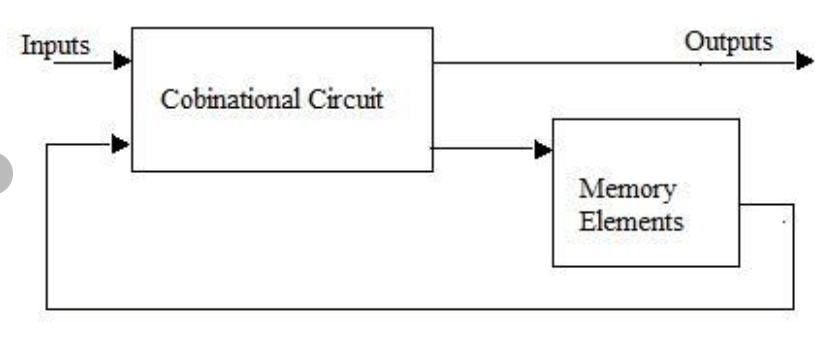
A Sequential circuit is a combinational logic circuit that consists of inputs variable (X), logic gates (Computational circuit), and output variable (Z). it produces an output based on current input and previous input variables (include memory elements).

Table 1:Sequential Circuits

## 2-Latches

* Latches are used for storing binary information.
* The output change in the Latches occurs at the clock level.

### 2.1- The SR (Set-Reset) Latch

#### 2.1.1- SR latch with NAND gates:

This circuit is active low set/reset latch, when S (set) input is 0 Q goes to1

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | ~Q |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 |

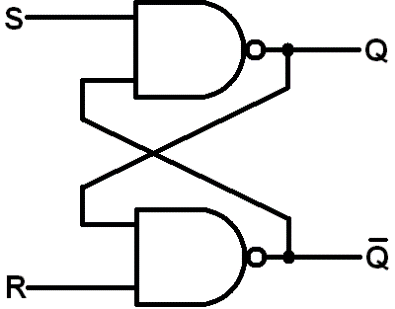
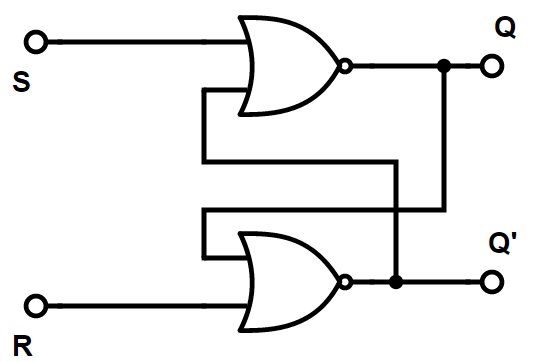


Table 2:SR latch with NAND gates Figure 1:SR latch with NAND gates

#### 2.1.2-SR latch with NOR gates: (Pre lab):

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | ~Q |
| 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |



R

S

Table 3:SR latch with NOR gates Figure 2:SR latch with NOR gates

#### 2.1.3- RS latch with control input:

|  |  |  |  |
| --- | --- | --- | --- |
| C | S | R | Next state of Q |
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | indeterminate |

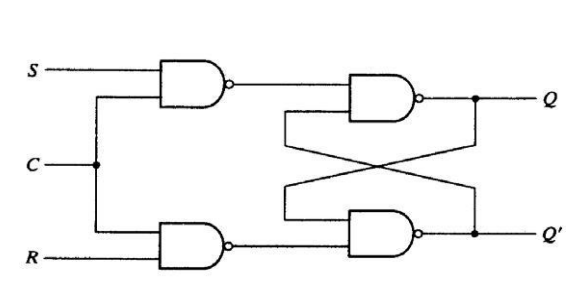


Table 4:RS latch with control input Table 5:RS latch with control input

### 2.2-The D Latch

|  |  |  |
| --- | --- | --- |
| C | D | Next state of Q |
| 0 | X | No change |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

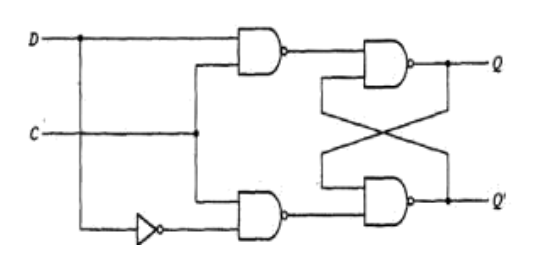


Table 6: D latch Figure 3:D latch

when D = 1 and EN = 1 the gated latch D flip-flop is ENABLE and SET (Q = 1) when D = 0 and EN = 1 the latch is ENABLE and RESET (Q = 0) but when EN = 0 the latch is DISABLE no question of SET REST. That means at EN = 0, any change in input D does not affect the output (No Change Condition).

## 3- Flip-Flops

* flip-flops are used for storing binary information
* The output change in the flip-flop occurs only at the clock edge

### 3.1-D Flip-Flop

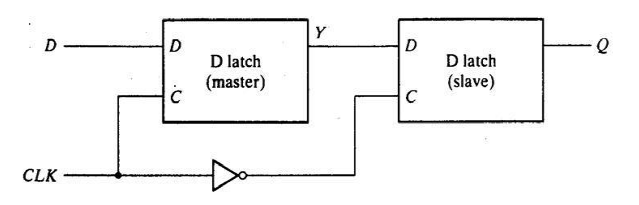


Figure 4:negative edge flip flop

|  |  |
| --- | --- |
| D | Q(t+1) |
| 0 | 0 |
| 1 | 1 |

characteristic equation:

Q(t+1) =D

Figure 5:D latch

### 3.2- JK Flip-Flop

|  |  |  |
| --- | --- | --- |
| J | K | Next state of Q |
| 0 | 0 | No change |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | ~Q |

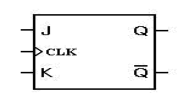


Table 7:JK Flip-Flop Figure 6:JK Flip-Flop

characteristic equation:

Q(t+1) =J.~Q(t)+ ~K. Q(t)

### 3.3-T Flip-Flop

|  |  |
| --- | --- |
| t | Next state of Q |
| 0 | Q |
| 0 | ~Q |



Table 8:T flip flop Figure 7:T Flip-Flop

## 4- Registers

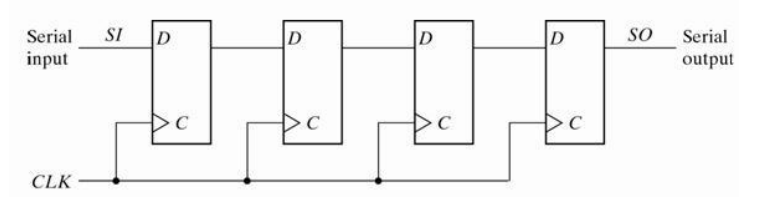
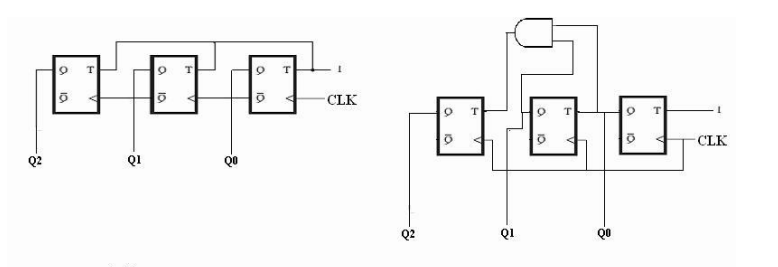
Is a collection of flip flops. A flip flop is used to store single bit digital data. For storing a large number of bits, the storage capacity is increased by grouping more than one flip flops. If we want to store an n-bit word, we have to use an n-bit register containing n number of flip flops.

Figure 8:: 4-bit Register

## 5- Counters

A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters.

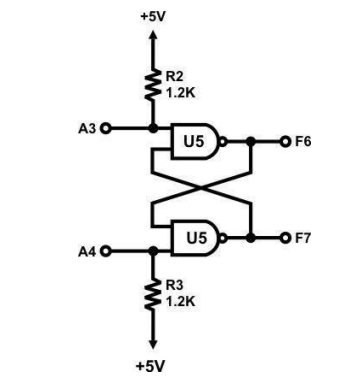
The counter is one of the widest applications of the flip flop. Based on the clock pulse, the output of the counter contains a predefined state. The number of the pulse can be counted using the output of the counter.

Figure 9:3-bit ripple counters Figure 10:3-bit synchronous counters

# PROCEDURE

## 1-Latches and Flip flops

### 1.1-Constructing RS latch with Basic Logic Gates

* Use IT-3008 module to construct the circuit shown in Figure1.
* Connect inputs A3, A4 to Pulser Switches SWA A (TTL), SWB B (TTL).
* Connect outputs F6 and F7 to Logic Indicators L1, L2.

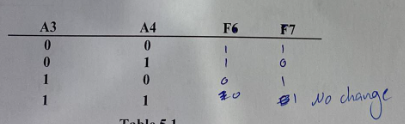
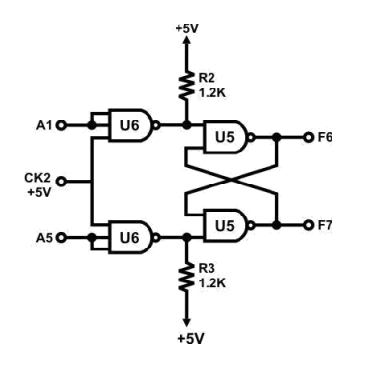


Table 9:RC latch

Figure 11:RS latch

### 1.2- Constructing RS latch with control input

* Use IT-3008 module to construct the circuit shown in Figure2.
* Connect inputs A1, A5 to Pulser Switches SWA A, SWB B
* Connect outputs F6 and F7 to Logic Indicators L1, L2.



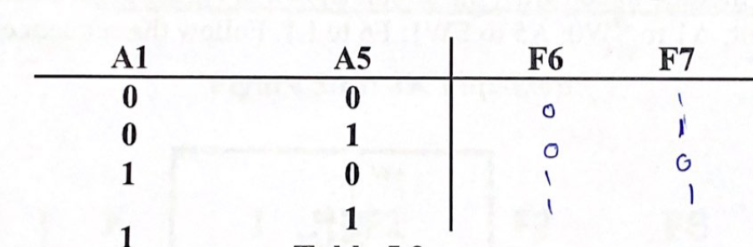
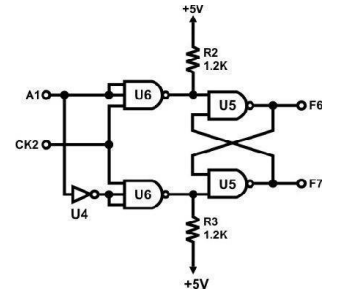


Table 10:RC latch with control

Figure 12:RC latch with control

The result is consistent with the theory.

### 1.3-Constructing D latch with RS latch

* Use IT-3008 module to construct the circuit shown in Figure3.
* Connect A1 to SW1; CK2 to SWA A and F6 to L1.

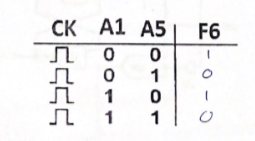
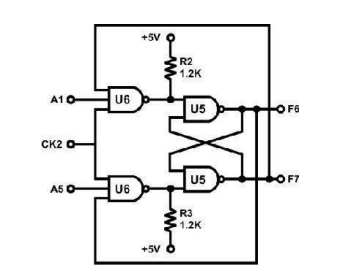


Table 11:D latch

Figure 13:D latch

### 1.4- Constructing JK latch with RS latch

* Use IT-3008 module to construct the circuit shown in Figure 4
* Connect CK2 to SWB B output; A1 to SW0; A5 to SW1; F6 to L1.

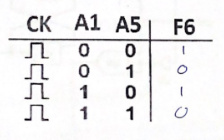
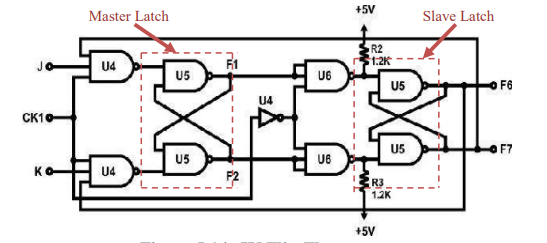


Table 12: JK latch with RS latch

Figure 14:JK latch with RS latch

## 2-Constructing JK Flip-flop with master- slave RS latches

* Use IT-3008 module to construct the circuit shown in Figure 5
* Connect CK2 to Pulser switch.
* Connect CK1 to SWA A output; J to SW1; K to SW0; F1, F2, F6, F7 to L3, L2, L1 and L0 respectively.

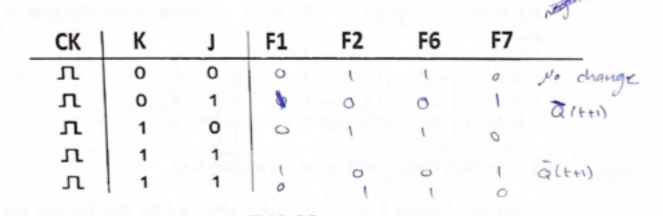


Figure 15:JK flip flop

Table 13:JK flip flop

This is a positive edge triggered flip flop

K =0 & j =0 give next state = present state

K =0 & j =1 give next state =0

K =1 & j =0 give next state =1

K =1 & j =1 give next state = ~present state

## 3- Registers

### 3.1- Constructing Shift Register with D Flip-Flops

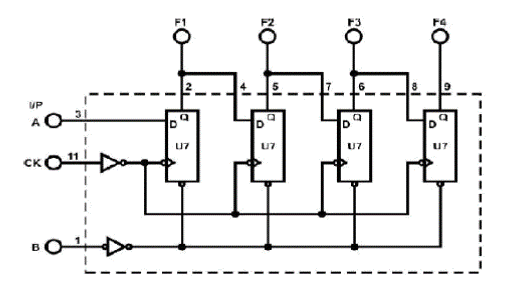
* Use Block Shift Register 1 of module IT-3008
* Connect B (clear) to SW0; A (I/P) to SW1; CK to SWA A output; F1, F2, F3, F4 to L1, L2, L3, L4 respectively.
* Set SW0 to “0” to clear B and then set SW0 to “1”.
* Follow the input sequence for A(I/P) below, and observe output display at F1, F2, F3 and F4:

1) at A= “1”, send in a CK signal from SWA

2) at A= “0”, send in a CK signal from SWA

3) at A= “0”, send in a CK signal from SWA

4) at A= “1”, send in a CK signal from SWA



Data (Serial-in to Parallel-out):

1. 1000
2. 0100
3. 0010
4. 1001

Its shift 1bit to right on each clock pulse.

### 3.2- 4-Bit Shift Register with serial and parallel load

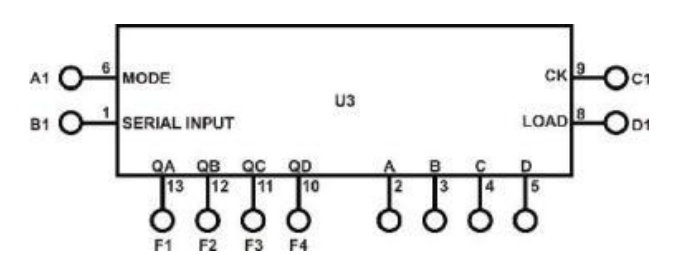
* Use Shift Register 2 module in IT-3008
* Connect Inputs A, B, C, D to SW0, SW1, SW2, SW3.
* Connect Outputs F1, F2, F3, F4 to L0, L1, L2, L3.
* Connect B1 (I/P) to DIP2.0 and A1 (MODE) to DIP2.1

Figure 16:shift register with serial and parallel load

* Connect CK (C1) to the clock generator TTL level output at 1Hz and change data at B1 with DIP2.0. Follow the input sequences for A1 in Table 5.7. Observe and record the outputs.

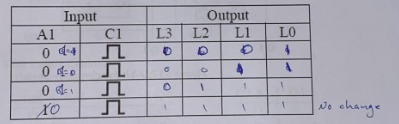


Table 14:4-Bit Shift Register with serial and parallel load

MODE is active low

* Connect LOAD (D1) to the clock generator TTL level output at 1Hz. Set A1 to “1”

 Table 15:4-Bit parallel load:

The data has been loaded correctly

## 4-Counters

### 4.1- 2-bit Synchronous Counter

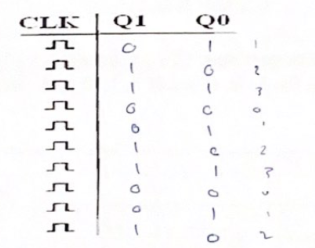
* Use IT-3007 module
* Connect CLK input to pulser switch.
* Connect counter outputs Q1 and Q0 to indication lamps.
* Apply clock pulses to CLK input

Table 16:: 2-bit Synchronous Counter

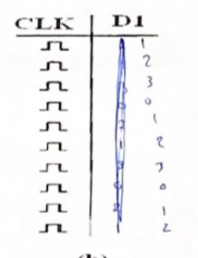
* Apply counter outputs Q1 and Q0 to seven segment display

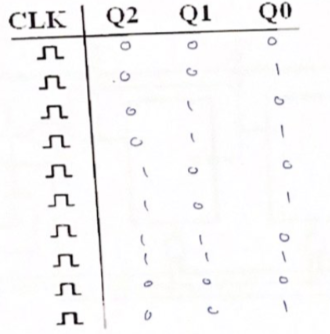
Table 17:2-bit Synchronous Counter

This counter counts from 1 to 3

### 4-2: 3-bit (divide-by-eight) Ripple Counter

* Use the IT-3007 module
* Connect CLK input to pulser switch.
* Connect counter outputs Q2, Q1 and Q0 to indication lamps.
* Apply clock pulses to CLK input
* Apply counter outputs Q2, Q1 and Q0 to seven segment display

Figure 17: 3-bit Ripple Counter



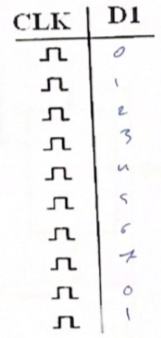


Table 18: 3-bit Ripple Counter

### 4.3- BCD Counter

* Use BCD counter (IC 7490) on IT-3008 module
* Connect C3, C4 to SW0 and SW1; D1, D2 to SW2 and SW3; F1~F4 to L1~L4, A2 to SWA A output; B2 to SWB B output.
* Connect F1 to B2, set C3, C4, D1 and D2 to ground and A2 to SWA A pulse. Measure and record the outputs F1, F2, F3, F4

Table 19:BCD counter

It should count from 0 to 9, but there was a glitch and we don't know why.

# Task 2:

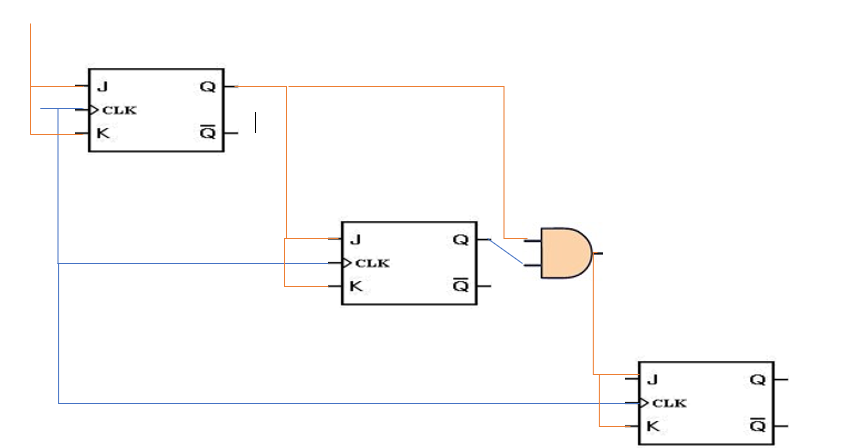
Modify the circuit in Figure 5.16 to be 3-bit Synchronous Counter.

Figure 18:3-bit Synchronous Counter.

# Task3:

change the connection of counter in Figure.19 to count from:

- 0-to-5

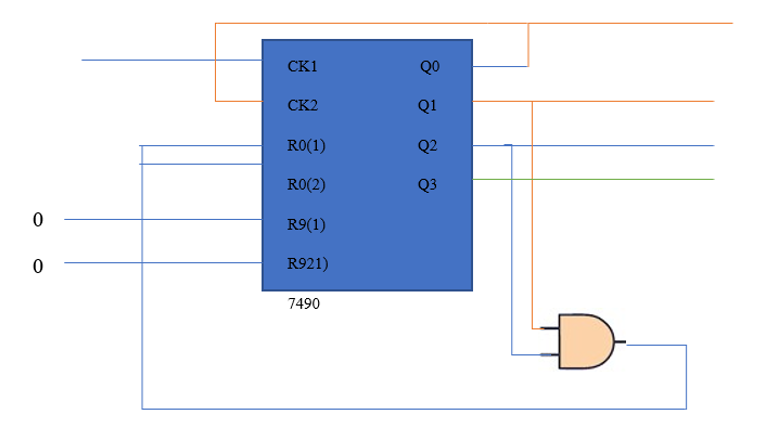


Figure 19:- 0-to-5 counter

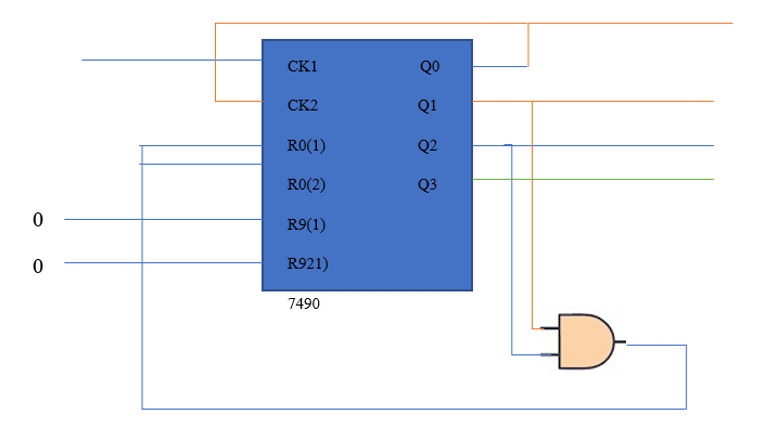
- 0-to-4

Figure 20::- 0-to-4 counter

# Conclusion

This experience clarified the concept of sequential circuits and memory unit (latches, flip-flop), The results of the experiment were as expected and nothing went wrong and It took two and a half hour.

# DISCUSSION

1. Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?

* latches tend to make glitches
* Analyzing of Latch circuits is difficult because of its level sensitive property.

2.What is the disadvantage of the RS flip flop?

Its output is undefined when both inputs are 1 (S=R=1).

3.What is the difference between “synchronous” and “ripple” counters?

Ripple Counter, different flip flops are triggered with different clock, not simultaneously. While in Synchronous Counter, all flip flops are triggered with same clock simultaneously and Synchronous Counter is faster than asynchronous counter in operation.

# References:

* <https://www.javatpoint.com/counters-in-digital-electronics>
* Digital Lab manual.
* <https://www.electrical4u.com/d-flip-flop-or-d-latch/>