

**Faculty of Engineering & Technology**

**Electrical & Computer Engineering Department**

**DIGITAL ELECTRONICS AND COMPUTER**

**ORGANIZATION LABORATORY - ENCS2110**

**Report #3**

**Experiment #7**

**Constructing Memory Circuits Using Flip−Flops**

**Prepared by: ID:**

Ro’a Nafi 1201959

**Partners:** Manar Shawahni 1201086

Leelyan Karajah1201191

**Instructor**: Dr. Ahmad Alyan  
**Assistant**: Mahmoud Hussain

**Section:** 13

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# Abstract

This experiment aims to Understand the basic structure of Random Access Memory (RAM) and test the circuit of 64-bit Random Access Memory (RAM).

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# Theory

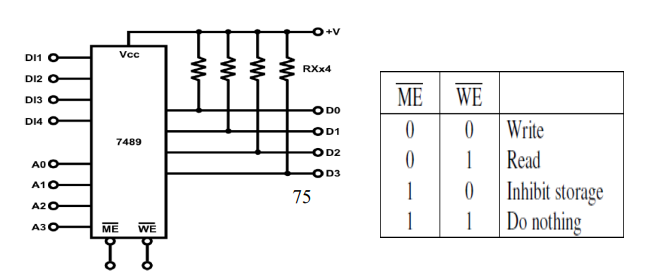
## 1. RANDOM ACCESS MEMORY (RAM)

Random access memory (RAM) is a computer's short-term memory, which it uses to handle all active tasks and apps, RAM is temporary storage that goes away when the power turns off .but It’s very fast memory.

There’re two types of RAMs:

* The Dynamic Random-Access Memory (DARM0
* The static Random-Access Memory (SRAM).

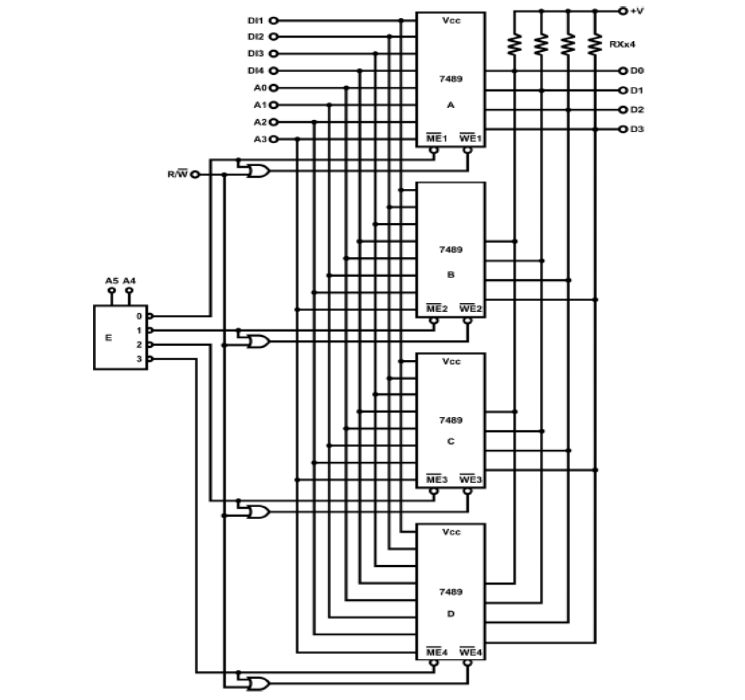
## 2.64-BIT RANDOM ACCESS MEMORY (RAM) CIRCUIT

in this memory there is 4 address lines, then 2^4 or 16 locations exist. A 4-bit data can be stored in each location, since the total capacity is 16×4, where the 4 is the number of data while 16 is the number of address lines.



*Figure 1:Block diagram of 16x4 RAM chip*

When ME' = 0 and WE' = 0, the memory is enabled, and the input process starts.



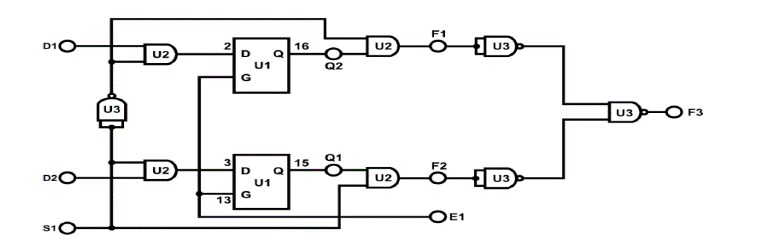
*Figure 2:Logical construction of a 6x4 RAM using four 4x4 RAMS*

When A4A5=00, A is selected, ME' and WE' of B, C and D all equal to “1”. Similarly, when A4A5=01, B is selected, ME' and WE' of C and D all equal to “1”. E is 2-4 decoders with “0” as its output. The unselected outputs are in high or “1” state. Since the outputs will have high impedance when ME' and WE' are both “1”, each R/W' control of 7489 are connected to an OR gate to ensure that when ME' = “1”, WE' will be equal to “1” too. When ME' = “0”, WE' is controlled by external R/W' control so that the “READ” operation is performed if R/W'= “1”. The “WRITE” operation is performed when R/W'= “0”.

# PROCEDURE

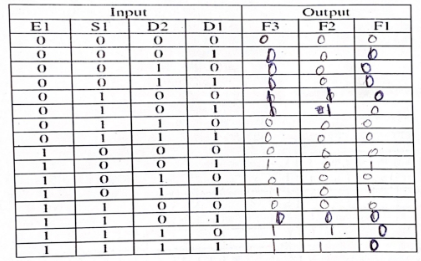
## Constructing Random Access Memory (RAM) with D Flip-Flop

* Using RAM block with D Flip-Flop of module IT-3011



*Figure 3:RAM block with D Flip-Flop of module IT-3011*

* Connect E1, S1, D2, D1 to Data Switch SW0~SW3 respectively.
* Connect outputs F1, F2, F3 to Logic Indicators L1~L3.



*Table 2:Extracted data observations and storing process of a 1x2 RAM*

### Task 1:

E1 =1 mean write, E1 =0 mean read.

* When E1=1, s1=0

F1=D1 & F2=0 & F3 = F1

* When E1=1, s1=1

F1=D1 & F2=D2 & F3 = F1 + F2

* When E1=0, s1=0

F1=0 & F2=0 & F3 = 0

* When E1=0, s1=1

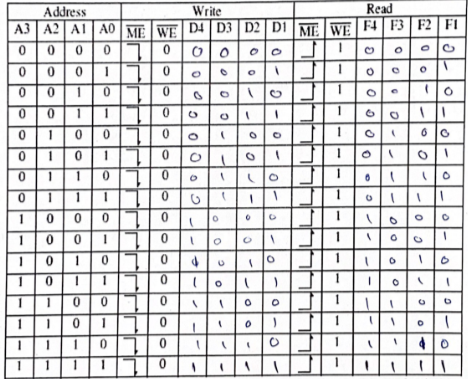
F1=0 & F2=~D2 & F3 = F2

## 2.RAM Memory 16\*4

* Using block RAM Circuit of module IT-3011.
* connect +5V, +15V of module IT-3011 to the +5V, 15V output of fixed power supply respectively.
* Connect inputs D4~D1 to DIP Switch 1.0~1.3; A3~A0 to DIP 2.0~2.3; S1 (ME) to Pulser Switch SWAA; S2 to Data Switch SW0. Outputs are indicated by CR1~CR4.
* Set SW0 (WE') to “0” for the “WRITE” task. Start from address 0000, input data to A0~A3 by setting the DIP switch. Activate SWA once to write the data into its assigned address. Repeat this process for all the addresses, ending with 1111. Record what was written into each address in Table 7.2 under the “WRITE” column.
* Now set SW0 (WE' ) to “1” for the “READ” task and connect S1 (ME' ) to Pulser Switch SWA

(Observe states of CR1~CR4 and record under the “READ” column)

* Disconnect SWA and “A” clip, then turn off the main power switch of IT- 3000 for about 10 seconds and turn it on again. Change address and press SWA then attempt to read the data.
* Disconnect “B” clip, VCC disappears. Repeat Step 5 to see if the data are still stored in the RAM



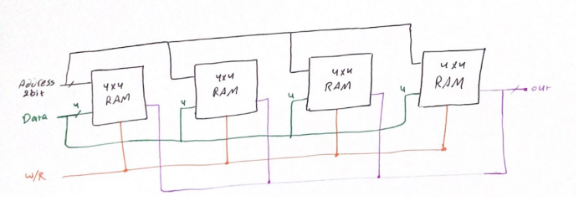
*Table 3: Extracted data observations and storing process of a 4x4 RAM*

* WE input represents the Read/Write signal input (reads the data from the address or write into it), ME represents the Enable input.
* Data bits are represented in D1 to   D4, address bits are represented in A1 to   A4.
* The memory worked correctly as it showed what was previously stored in it as noticed in

the table

# Post lab

* Problem 1: Design a 4x16 RAM using four 4x4 RAMS.



*Figure 5: 4x16 RAM using four 4x4 RAMS.*

* Problem 2: Although D latches are useful for storing binary information, they are not used in RAM circuit design, why?

Latches are prone to glitches which are unwanted in the design. In addition, the latches are level triggered which means the change will occur at the change of any enable signal.

# Conclusion

The RAM memory is a volatile storage element that doesn't keep the data after removing the power supply and is used for storing the operating system, applications and other data temporary.

Each RAM memory has various capacities depending on the number of address lines and it can be accessed only by these addresses.

# References

* [avast](https://www.avast.com/c-what-is-ram-memory)
* Digital Lab manual.