

ENCS2110

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

Pre-Lab Experiment #5

Sequential Logic Circuits

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# The SR (set – Reset) Latch



Figure 1: SR latch with NAND gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S | R | Q | Q’ |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 1 | 0 | 1 | After S = 1, R = 0 |
| 0 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 0 | After S = 0, R = 1 |
| 0 | 0 | 1 | 1 |  |



Figure 2: RS latch with control input

|  |  |  |  |
| --- | --- | --- | --- |
| C | S | R | NEXT STATE OF Q |
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | Q = 0 Reset state |
| 1 | 1 | 0 | Q= 1 set state |
| 1 | 1 | 1 | Indeterminate |



Figure 3: D-Latch

|  |  |  |
| --- | --- | --- |
| C | D | Next state of Q |
| 0 | X | No Change |
| 1 | 0 | Q = 0 Reset state |
| 1 | 1 | Q = 1 Set state |

