

ENCS2110

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

Experiment 7: Constructing Memory Circuit Using Flip-Flop

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# Abstract

This experiment aims to examine the 64-bit RAM and how to construct a memory using flip-flops, due to the corona pandemic we used the Proteus software.

# Theory

## Random Access Memory (RAM)

Random Access Memory is a type of computer memory which can be accessed randomly, the RAM is volatile which means the data is stored in memory as long as the computer power is on, so the moment the power is off all the data will be lost, due to that the RAM is used in immediate work since it’s fast, there’s two types of RAMs: The Dynamic Random-Access Memory (DARM), the other type is the static Random-Access Memory (SRAM).

## Read Only Memory (ROM)

This memory is a read-only type of memory, it can’t be changed, also it stores data permanently and not-volatile which means it stores the data and won’t get removed when the power is off (ROM will held the data), usually is type of memory is used to hold major programming data, beside the tasks needed to start the PC or any program, there are some types of ROM: programmable read-only memory (PROM), erasable programmable read-only memory (EPROM).

## The Main Memory

It’s the storage space in the computer, which is divided into cells (separate locations), each one of them has a unique address, there are many types of data storages that are used in a computer such as RAM and ROM that were mentioned before.

# Procedure, Data and results

## Constructing Random Access Memory (RAM) with D Flip-Flop

The circuit was designed as shown in Figure 1



Figure : RAM with D Flip-Flop

|  |  |
| --- | --- |
| Input | Output |
| E1 | S1 | D2 | D1 | F3 | F2 | F1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Table : Output of RAM

## RAM Memory 16\*4 using the IC 7489



Figure : RAM block using IC 7489

|  |  |  |
| --- | --- | --- |
| Address | Write | Read |
| A3 | A2 | A1 | A0 | ME | WE | D4 | D3 | D2 | D1 | ME | WE | F4 | F3 | F2 | F1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

As shown in the figure, the Data bits are represented in D1 D4, while the address bits are represented in A1 A4, where the previous data should be stored, meanwhile the WE input represents the Read/Write signal input, and finally ME represents the Enable input.

 AS noticed in the table, when the circuit is enabled, it reads the data from the address or write into it depending on the state of the WE signal.

## 64-bit Random Access Memory (RAM) circuit



Figure 3: 64-bit RAM

# Conclusion

In conclude, the RAM is the volatile & temporary memory of the computer, in this experiment the RAM was investigated through different circuits on Proteus, finally the simulation went well and had shown the basic operations of RAM.