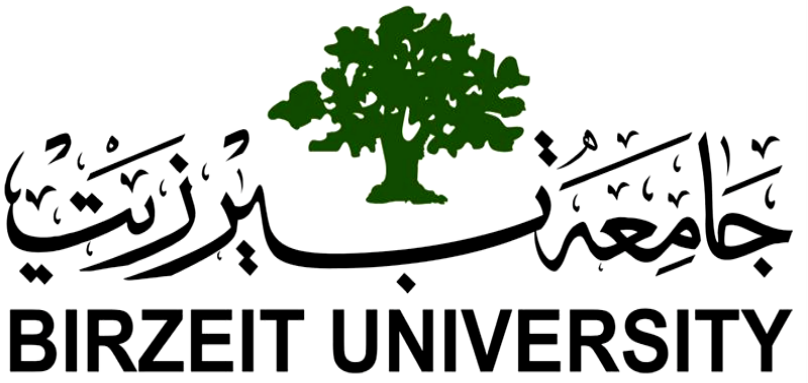

Faculty of Engineering & Technology
Electrical & Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY - ENCS2110

Report #1

Comparators, Adders and Subtractors

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Section: 5
Date: 28/09/2020

Abstract

The aim of this experiment is to understand and see how digital comparators work, after that this experiment will present the way of constructing 1-bit comparator using basic logic gates such as: NAND, NOR, XOR, XNOR etc. and IC.

In addition, this experiment contains enough information about implementing (using basic logic gates) Half-Adder which is a digital circuit has 2-bit input and 2-bit output: the sum of the inputs and the carry of them. Also there is the Full-Adder which works exactly as the Half-Adder but it has 3-bit input, so it is able to give the sum and the carry of 3 bits, the additional bit input from the Half-Adder is to give the adder the ability of adding a carry from previous addition operation.

Finally, the last major aim of this experiment is to understand how the complements work, and use the theory of complements to implement Half- and Full-Subtractor circuits, which work in a similar way to Half- and Full-Adder but they give the difference of 2 or 3 bits and the borrow.

Another thing to mention is the experiment shows how to construct 4-bit adders which has 8-bit inputs and gives the sum of two 4-bit binary numbers, and BCD adder which gives the sum of two BCD numbers. Also the constructing of 4-bit Subtractor is given in the experiment.

Contents

Theory

The experiment includes: comparator, half adder, full adder, 4-bit adder, BCD adder, half subtractor, full subtractor and 4-bit subtractor. In this part we will explain how each circuit work and the implementation of some of the circuits using basic logic gates.

i. Comparator

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number [1].

A 1-bit comparator has 2 inputs, each of them is 1-bit binary number and the there is 3 outputs to tell the result of comparing the first number to the second number. Figure 1 shows the implementation of 1-bit comparator using basic logic gates, and Figure 2 shows the block diagram of 1-bit comparator.

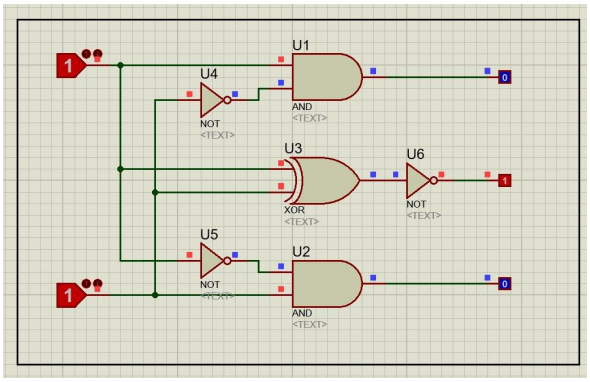

Figure 1: Comparator Logic Diagram.

The equation of (A > B) is AB' and the equation of (A < B) is A'B and the equation of (A=B) is (A⊕B)'.

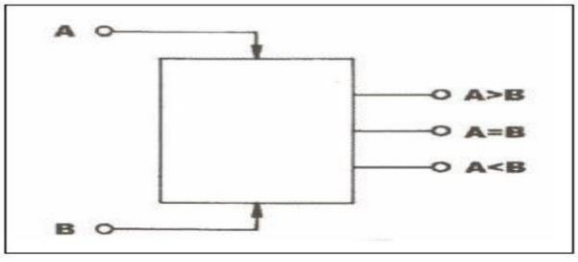

Figure 2: Comparator Circuit Symbol

ii. 4-bit Comparator

In actual applications 4-bit comparators are used most often. In a 4-bit comparator, each bit represents 20, 21, 22 and 23. Comparison will start from the most significant bit (23), if input A is greater than input B at the 23 bit, the “A>B” output will be in high state. Figures 3 and 4 show the schematic and symbol of 4 bit comparator [2]

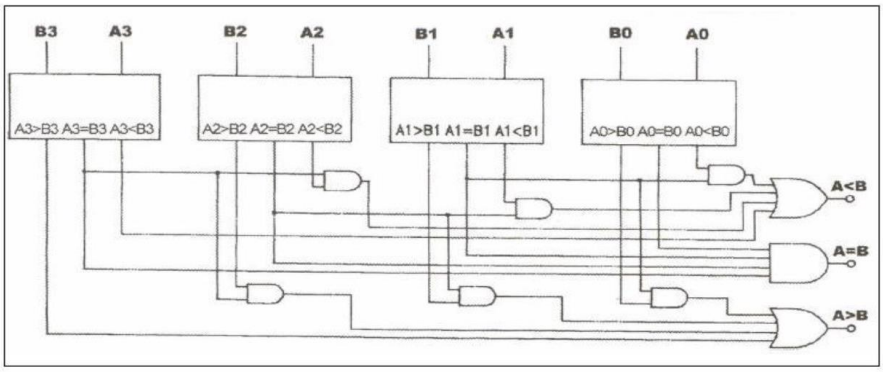

Figure 3: 4-bit Comparator Circuit Symbol

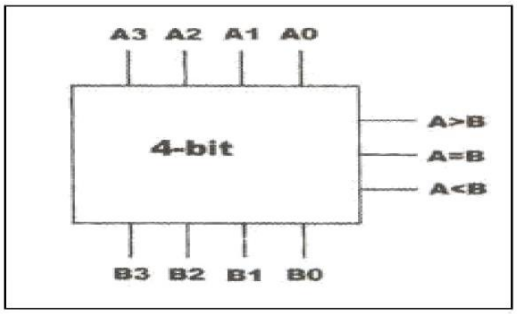

Figure 4: 4-bit Comparator Circuit Symbol

iii. Half-Adder

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output [3]. If x and y are the input bits, then the equations of the sum (S) and the carry (C) is as the following.

$S = x \oplus y$

$C = xy$

Figure 3 shows the truth table of the Half-Adder and the implementation of it using basic logic gates.

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

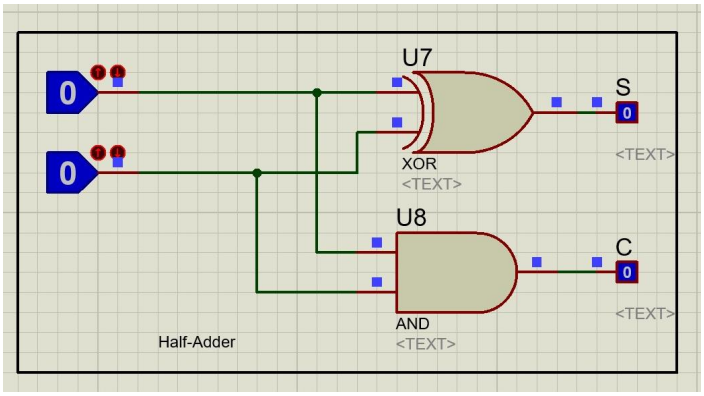

Figure 5: Half-Adder Truth Table and Logic Diagram.

iv. Full-Adder

Full-Adder is a combinational logic circuit that works as the half-adder but it has 3 inputs, and the circuit provides the sum (S) of the 3 inputs and the carry (C) from the operation. If the inputs was x, y and z, then the sum and the carry is given by the following equations.

$S = (x \oplus y) \oplus z$

$C = xy + xz + yz$

Figure 4 shows the truth table of the full-adder and the implementation using basic logic gates.

Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

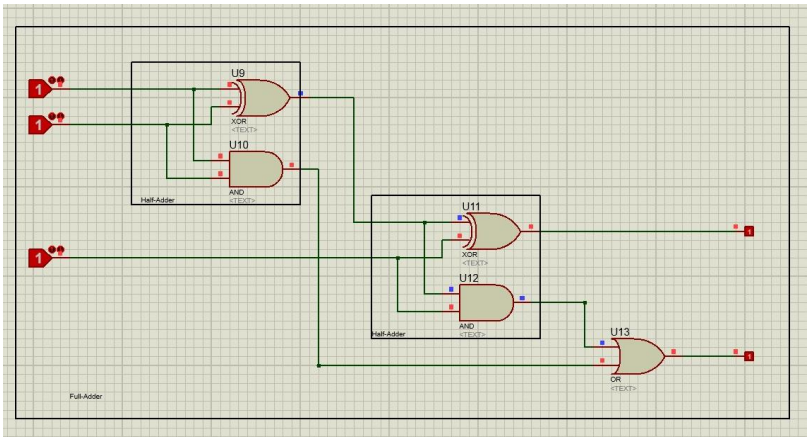

Figure 6:Full-Adder Truth Table and Logic Diagram.

v. Half-Subtractor

The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend A and subtrahend B and two outputs the difference D and borrow out Bout The borrow out signal is set when the subtractor needs to borrow from the next digit in a multi-digit subtraction. That is, Bout = 1 when A < B. Since A and B are bits, Bout = 1 if and only if A = 0 and B = 1. The equation of D and Bout is as following.

$S1 = A \oplus B$

$C1 = A'B$

Figure 5 shows the truth table and the implementation of Half-Subtractor using basic logic gates.

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

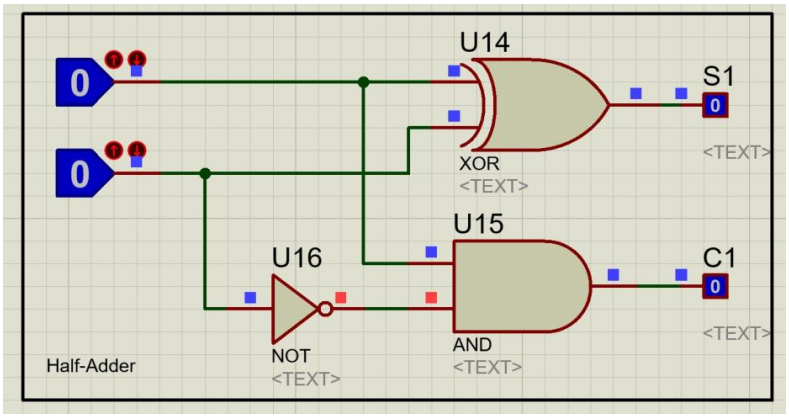

Figure 7: Half-Subtractor Truth Table and Logic Diagram.

vi. Full-Subtractor

Full-Subtractor is a combinational circuit which is used to perform subtraction of two bits. It works in a similar way of the half-subtractor. If the 3 bits we want to get difference of are X, Y, Bin then the difference D and the borrow Bout are given as the following equations:

$D = X \oplus Y \oplus B_{in}$

$B_{out} = X'B_{in} + X'Y + YB_{in}$

Figure 6 shows the truth table and the implementation of Full-Subtractor using basic logic gates.

Inputs			Outputs	
X	*Y*	B_{in}	*D*	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

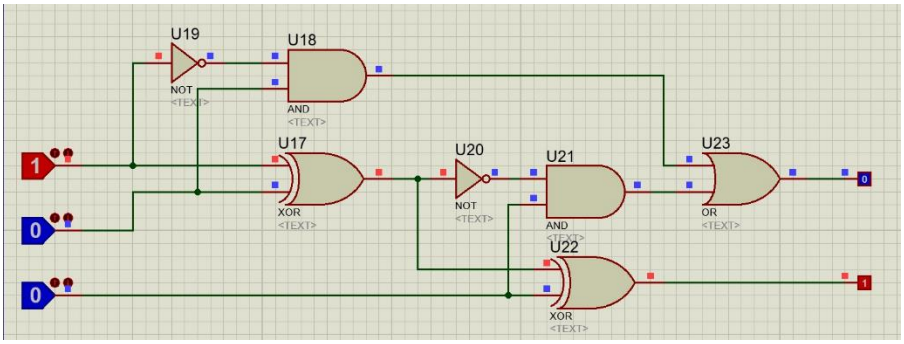

Figure 8: Full-Subtractor Truth Table and Logic Diagram.

vii. BCD-Adder

A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum BCD digit and a carry out bit. The maximum number in BCD is 9, if it is more than 9 adding 6 to the result.

Figure shows the logic diagram of BCD that takes 2 number 4-bit and find the summation, then if the result is more than 9, it will add 6. using 4-bit binary adder and some of basic gates as you see in the figure .

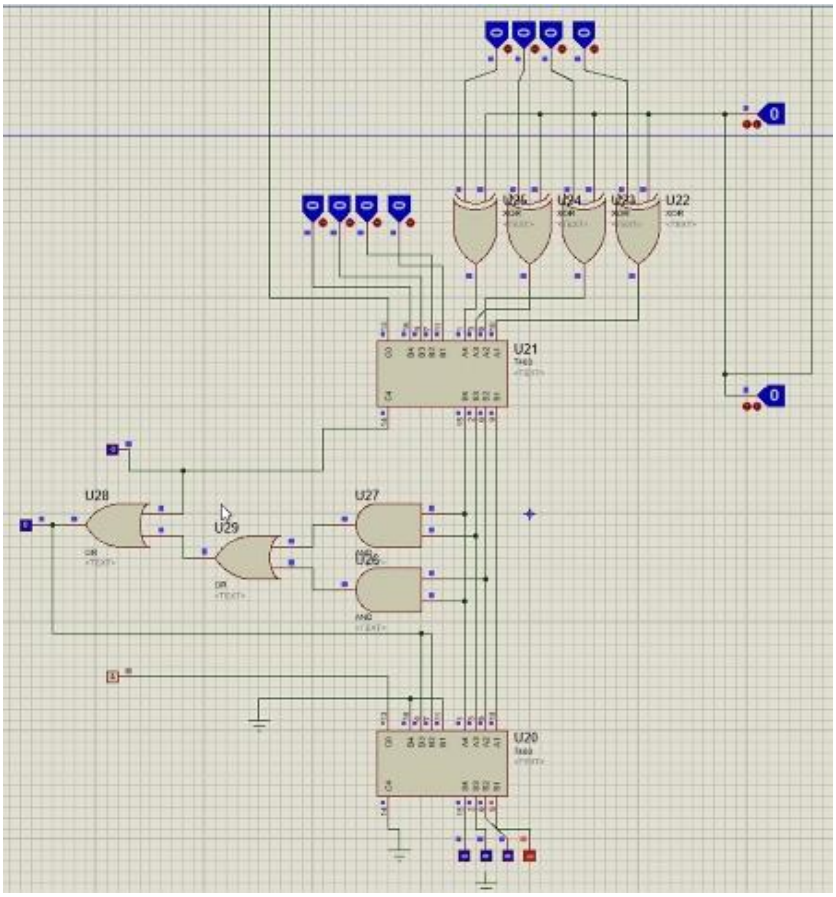

Figure 9: BCD-Adder Logic Diagram.

Procedure & Discussion

The logic diagram was designed using Protues software as follow:

i. Comparator:

AND, XOR and NOT gates used to design comparator. In Protues, LOGICSTATE and LOGICPROBE also used to represent the inputs and outputs as shown in figure below.

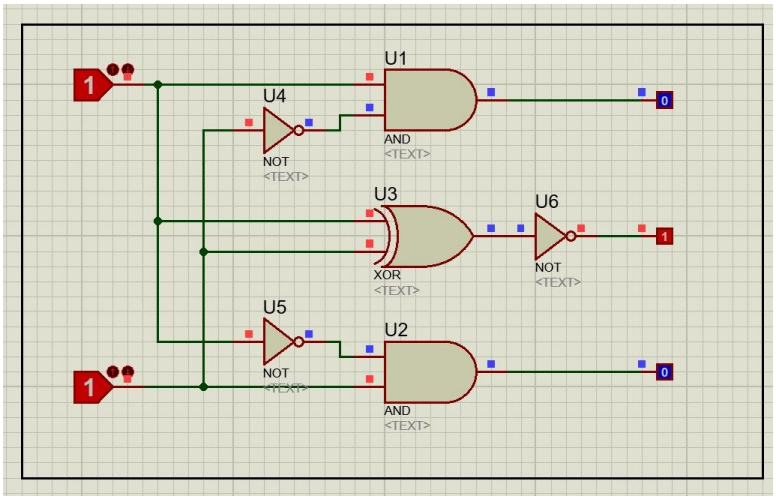

Figure 10: Comparator Logic Diagram.

The table below shows the inputs and the outputs of comparator.

Table 1: Comparator Truth Table

Inputs			Outputs		
A	B		F1 (A>B)	F2 (A=B)	F3 (A<B)
0	0	A=B	0	1	0
1	0	A>B	1	0	0
0	1	A<B	0	0	1
1	1	A=B	0	1	0

ii. Half-Adder

XOR, AND gates, LOGICSTATE and LOGICPROBE used to design Half-Adder.

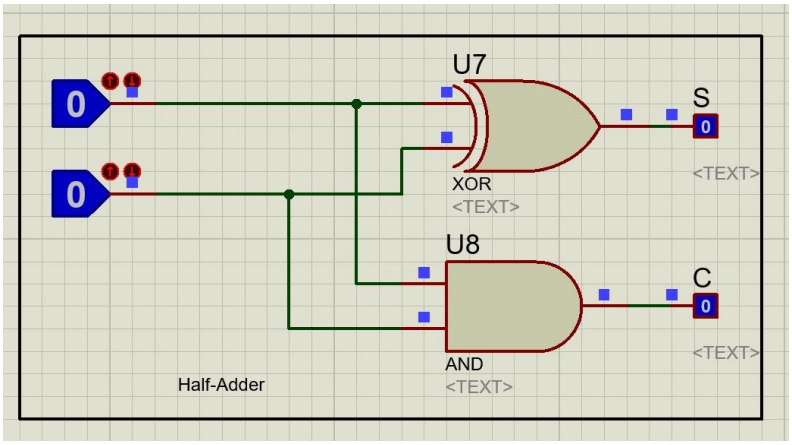

Figure 11: Half-Adder Logic Diagram.

And this is the truth table of the Half-Adder

Table 2: Half-Adder Truth Table

Inputs		Outputs	
A	B	C (Carry)	S (Sum)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

iii. Full-Adder

Full-Adder designed using two Half-Adders and one OR gate. It has 3 inputs and 3 outputs.

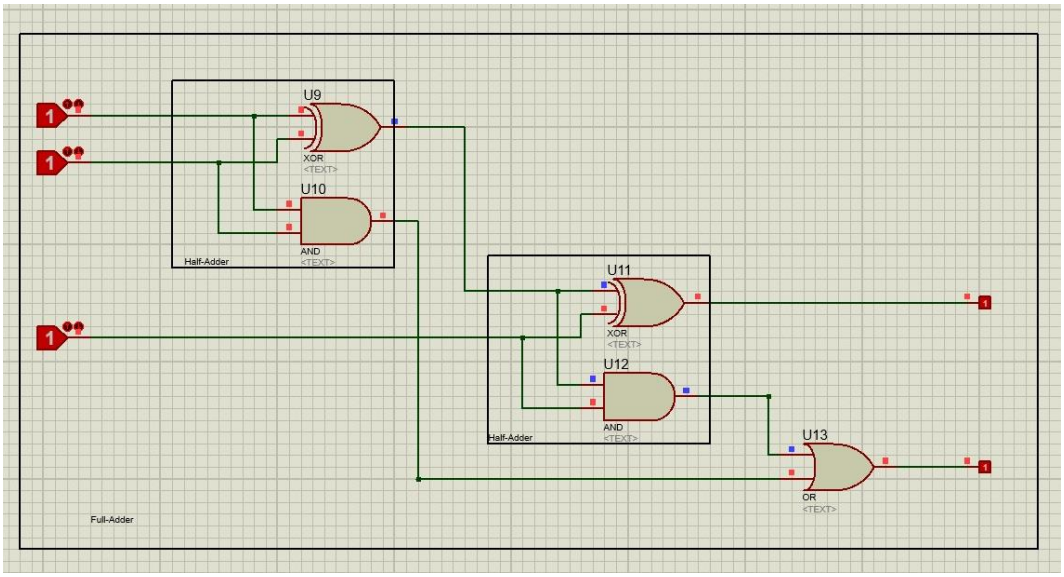

Figure 12: Full-Adder Logic Diagram.

Table 3: Full-Adder Truth Table

Inputs			Outputs	
C	B	A	C (Carry)	S (Sum)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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iv. 4-bit Full-Adder

Using four 4-bit Full-Adders to make 4-bit Full-Adder as shown below.

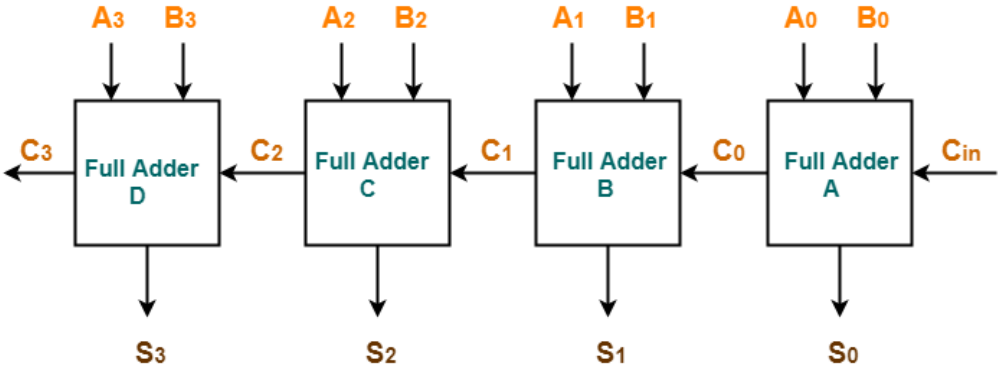


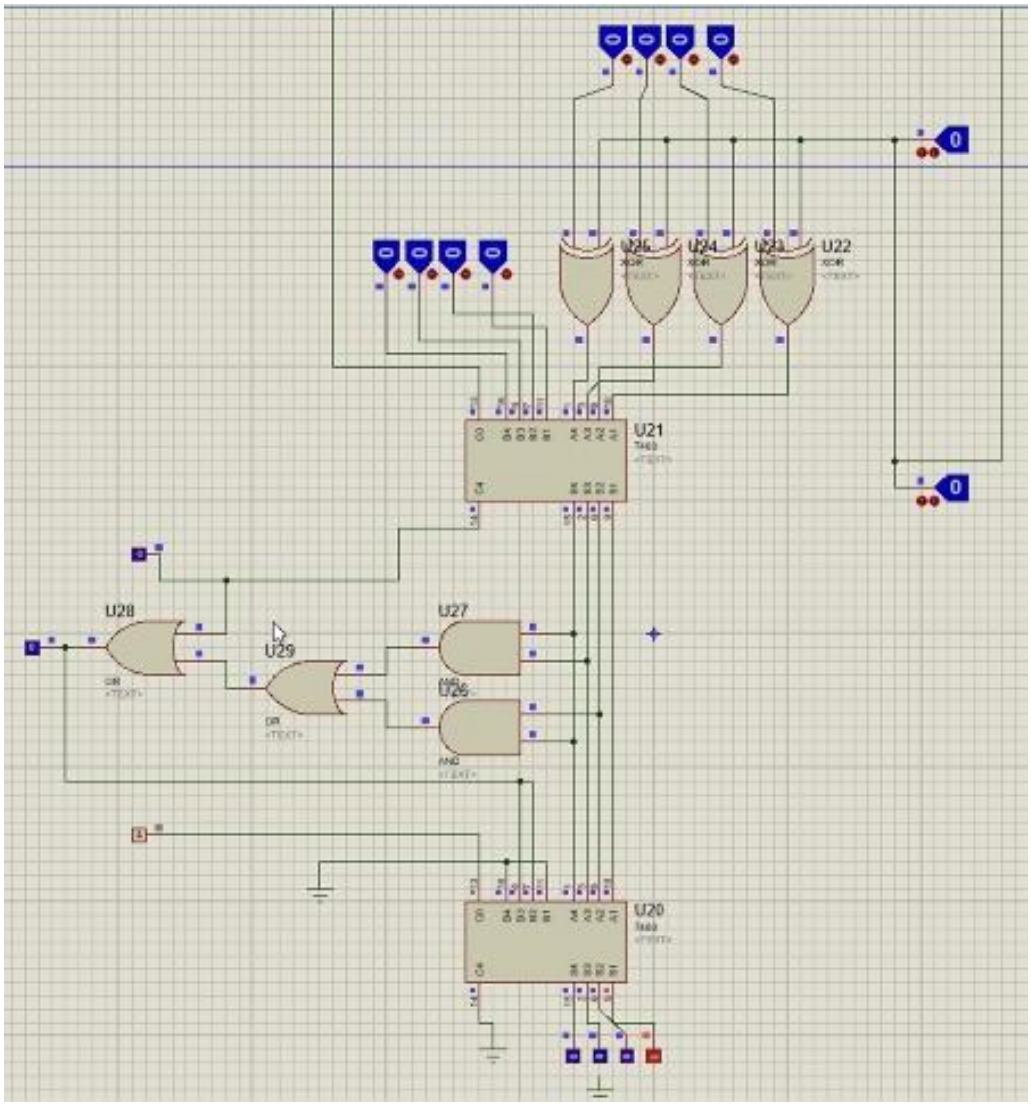
Figure 13: 4-bit Full-Adder Logic Diagram [4]

Table 4: 4-bit Full-Adder Truth Table

INPUT								OUTPUT				
Y3	Y2	Y1	Y0	X3	X2	X1	X0	(Carry)				
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	1	1	0	0	0	1	1	0
0	0	0	0	1	0	0	1	0	1	0	0	1
0	0	0	0	1	1	1	1	0	1	1	1	1
0	0	0	1	0	0	1	1	0	0	1	0	0
0	0	0	1	0	1	1	0	0	0	1	1	1
0	0	0	1	1	0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0	0	1	0	0	1
0	1	0	0	1	0	0	0	0	1	1	0	0
0	1	0	0	1	1	1	1	1	0	0	0	0
1	0	0	0	0	1	1	1	0	1	1	1	1
1	0	0	1	1	0	0	1	1	0	0	1	0
1	0	1	0	1	0	1	1	1	0	1	0	1

v. BCD-Adder

A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum BCD digit and a carry out bit. The maximum number in BCD is 9, if it is more than 9 adding 6 to the result.



We notice that when any of the two numbers is more than 9 in decimal, the bcd adder adds 6 in binary so the answer can be true.

vi. Half-Subtractor

Half Subtractor is used for subtracting one bit from another single bit. The truth table of Half Subtractor is shown below.

Table 5: Half-Subtractor Truth Table

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The logic diagram explains in figure 14

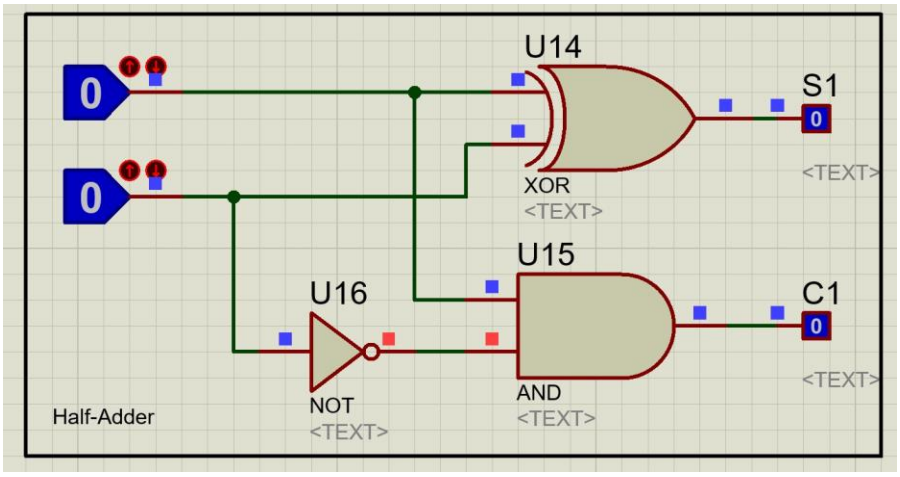


Figure 14: Half-Subtractor Logic Diagram

vii. Full-Subtractor

Full-Subtractor is used to perform subtraction of two bits.

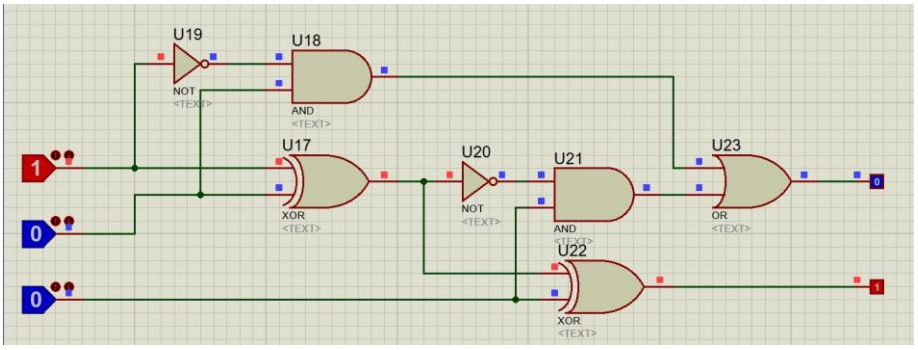


Figure 15: Full-Subtractor Logic Diagram

Table 6: Full-Subtractor Truth Table [5]

Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

viii. 4-bit Full-Subtractor

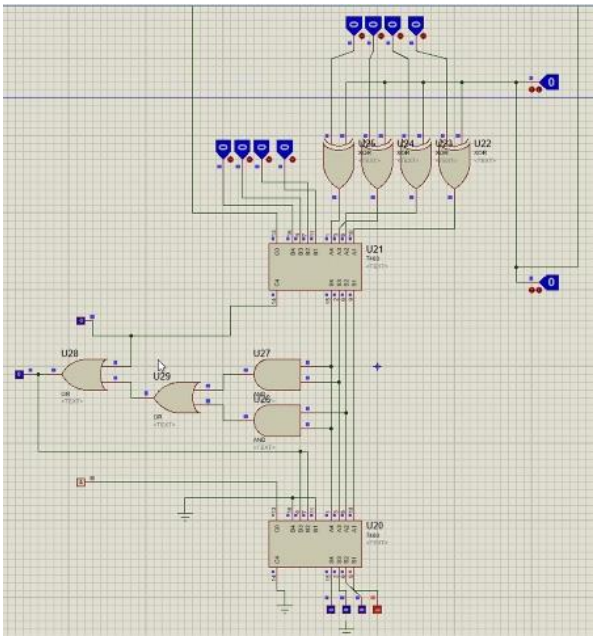


Figure 16: 4-bit Full-Subtractor

Table 7: 4-bit Full-Adder Truth Table

INPUT								OUTPUT				
Y3	Y2	Y1	Y0	X3	X2	X1	X0	F1	F11	F10	F9	F8
0	1	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	1	1	0	0	0	1	0
1	0	0	0	0	0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	1	0	1	1	1	0
1	0	0	1	1	0	0	0	0	0	0	1	0
1	0	0	1	0	1	1	1	0	0	1	0	0
1	0	1	0	0	1	1	0	0	1	0	0	0
1	0	1	0	0	1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	1	1	0	1	1	0	0

Conclusion

Comparators, adders and subtractors are digital circuits which can be implemented easily using basic logic gates. Full-adders and full-subtractors can be implemented using half-adders and half-subtractors, also we can use a 1-bit comparator, adder and subtractor to build an n-bit comparator, adder and subtractor. We can notice that these components are flexible enough to give us the ability of making an n-bit component from them easily.

In addition, we can conclude from the experiment that we can think of a way to design a circuit for multiple use, such as 4-bit adder-subtractor. We could transform a 4-bit adder into 4-bit subtractor only by changing an input, and for sure we don’t forget to mention that we needed some extra gates to be able to design the mentioned multiple circuit, for example we needed a 4 XOR gates to design the 4-bit adder-subtractor.

References

[1] https://en.wikipedia.org/wiki/Digital_comparator. Accessed on 28/09/2020 at 02:21AM.

[2] ENCS211 Lab Manual. Accessed on 28/09/2020 at 04:32AM.

[3] http://www.circuitstoday.com/half-adder. Accessed on 28/09/2020 at 07:12PM.

[4] https://www.gatevidyalay.com/ripple-carry-adder/. Accessed on 28/09/2020 at 09:46PM

[5] https://www.watelectronics.com/full-subtractor-circuit-diagram-using-basic-gates-and-applications/. Accessed on 28/09/2020 at 09:52PM