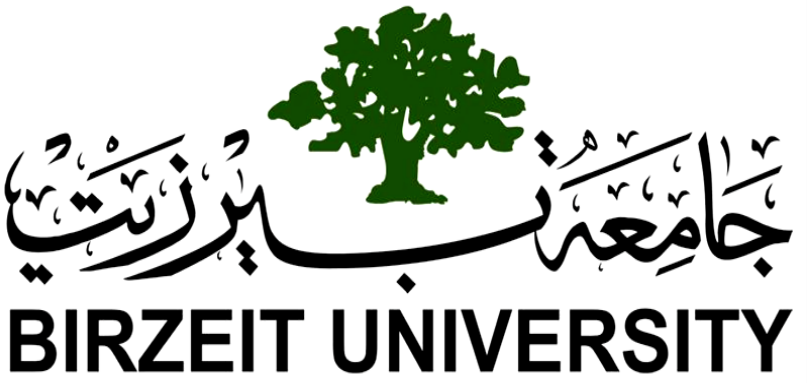

Faculty of Engineering & Technology
Electrical & Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY - ENCS2110

Report #3
Sequential Logic Circuits

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Section: 5
Date: 10/10/2020

Abstract

Doing arithmetic or logical operations is not sufficient for a system, data or results need to be stored.

Here we examine the basic gates for storing only one bit that can be made to store lots of data, these gates make up devices called latches, flip flops, counters, and registers.

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Theory

Sequential logic circuits are those, whose output depends not only on the present value of the input but also on previous values of the input signal (history of values) which is in contrast to combinational circuits where output depends only on the present values of the\ input, at any instant of time. Sequential circuit can be considered as combinational circuit with feedback circuit.[1]

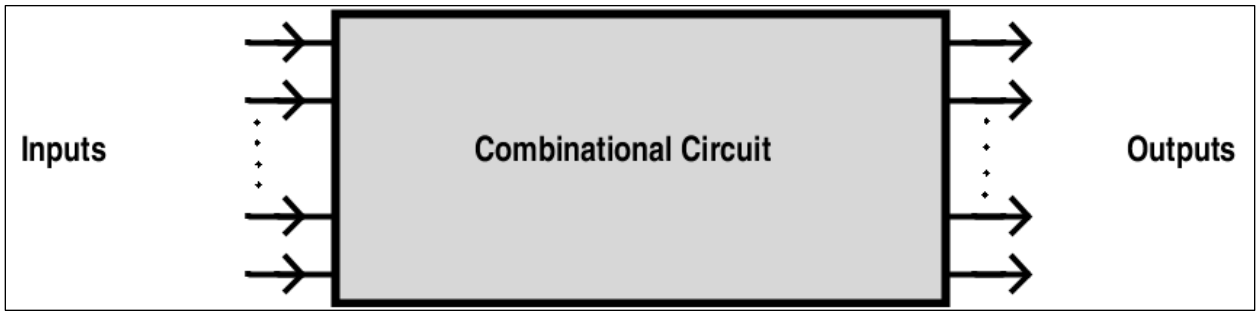


Figure 1 - Combinational Logic Circuits

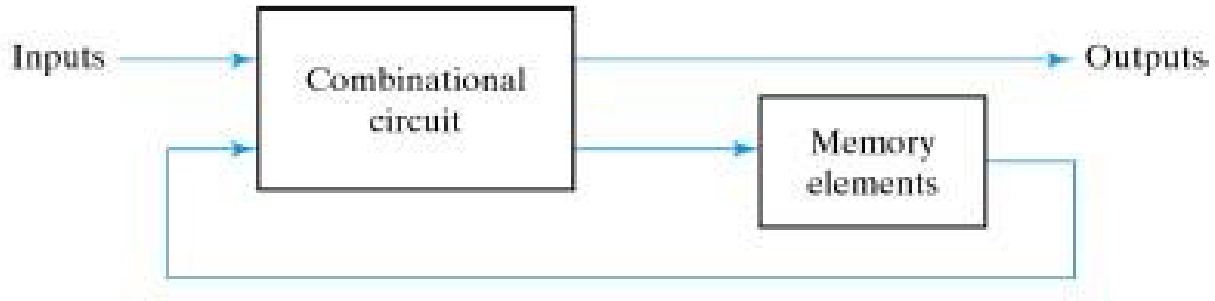


Figure 2 - Sequential Logic Circuits

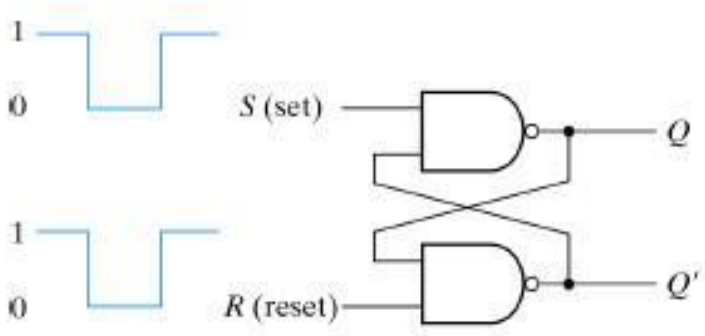
LATCHES

The majority of applications of digital logic require the storage of information. For example, a circuit that controls a combination lock must remember the sequence in which the digits are dialed in order to determine whether to open the lock. Another important example is the storage of programs and data in the memory of a digital computer. The basic electronic element for storing binary information is called a latch.[2]

Latch is an electronic logic circuit with two stable states i.e. it is a bistable multivibrator. Latch has a feedback path to retain the information. Hence a latch can be a memory device. Latch can store one bit of information as long as the device is powered on. When enable is asserted, latch immediately changes the stored information when the input is changed i.e., they are level triggered devices. It continuously samples the inputs when the enable signal is on.[3]

SR Latch

An SR latch has one job: set or reset. It can be implemented using NOR gates or NAND gates. Using NOR gates it'd be active high, but using NAND gates it'd be active low.



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

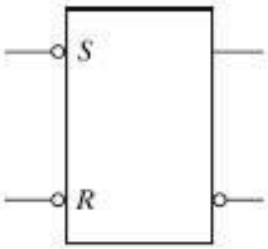
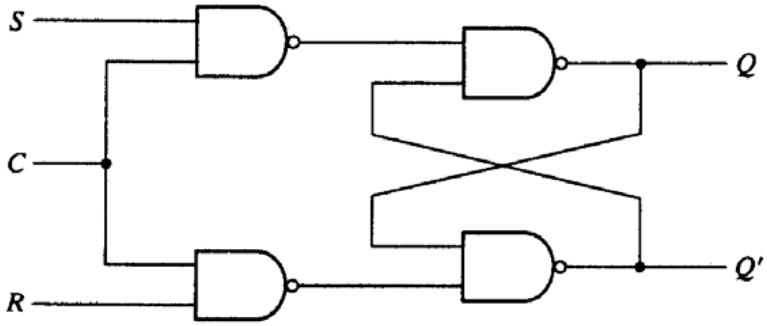


Figure 3: SR latch with NAND gate

Gated SR Latch (control input)

Generally, latches are transparent i.e. the output changes immediately when there is a change in the input. But for many applications, it is desirable to have an isolated period where the output doesn't change even when there is a change in the input. During this period, the outputs are said to be truly 'latched'. This can be achieved with the use of an extra input (enable or clock or gate). If the enable (or clock or gate) signal is not asserted, the inputs are ignored and the outputs are latched to the previous values. In order to use this extra signal, additional logic should be added. These circuits are called Gated or Clocked Latches.[4]

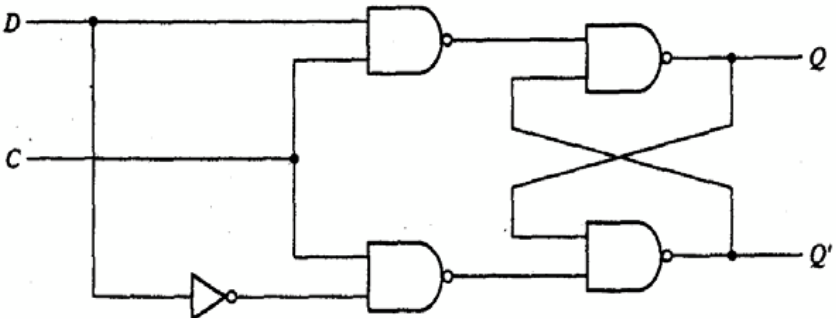


C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

Figure 4: Gated SR Latch Logic Diagram and Truth Table

D Latch

The race around condition in SR latch that occurs when S = R = 1 can be avoided in D latch as the R input is replaced with inverted S which is renamed to D. hence there are no illegal or forbidden inputs. In a D latch, Q always D.[5]



C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

Figure 5: D-Latch Logic Diagram and Truth Table

FLIP FLOPS

The term flip-flop refers to a storage element that changes its output state at the edge of a controlling clock signal. A flip-flop is said to be edge triggered if data present at the input are transferred to the output only at a transition in the clock signal. The input and output are isolated from each other at all other times. The terms positive (leading) edge triggered and negative (trailing) edge triggered describe flip-flops in which data transfer takes place at the 0-to-1 and the 1-to-0 clock transitions, respectively. For proper operation, edge-triggered flip-flops require the triggering edge of the clock pulse to be well defined and to have a very short transition time.

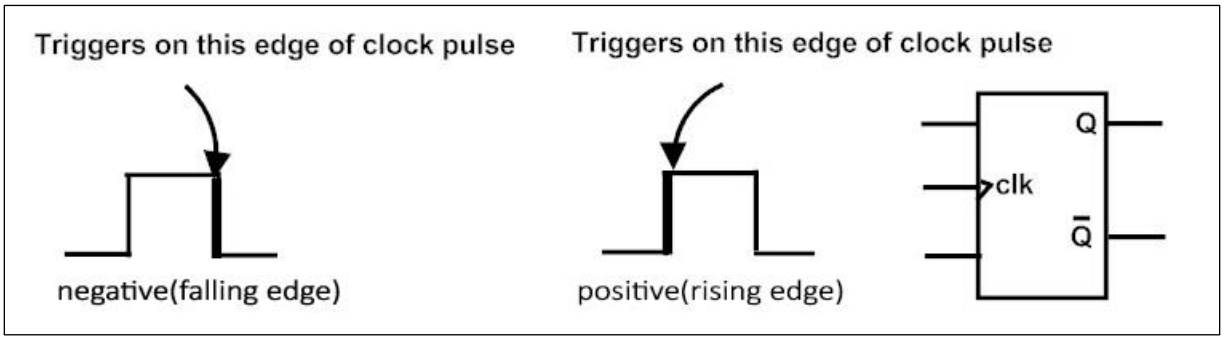


Figure 6 - Edge Triggered

The state of a flip-flop is determined by its present state and the logic values on its input terminals. Sometimes it is desirable to force a flip-flop into a particular state, either 0 or 1, regardless of its present state and the values of the normal inputs. For example, when a computer is powered on, it is necessary to place all flip-flops into a known state. Usually, this means resetting their outputs to state 0. In some cases, it is desirable to preset some flip-flops into state 1.[6]

D Flip Flop

A D flip flop is designed using two D latches (master and slave).

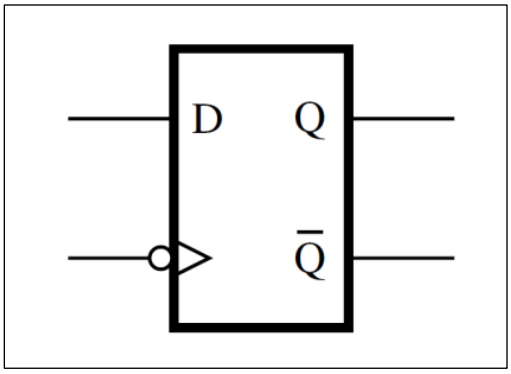


Figure 7 - D Flip Flop Block Diagram

A D flip flop can be negative or positive edge triggered, here in this example is a positive edge triggered D Flip Flop.

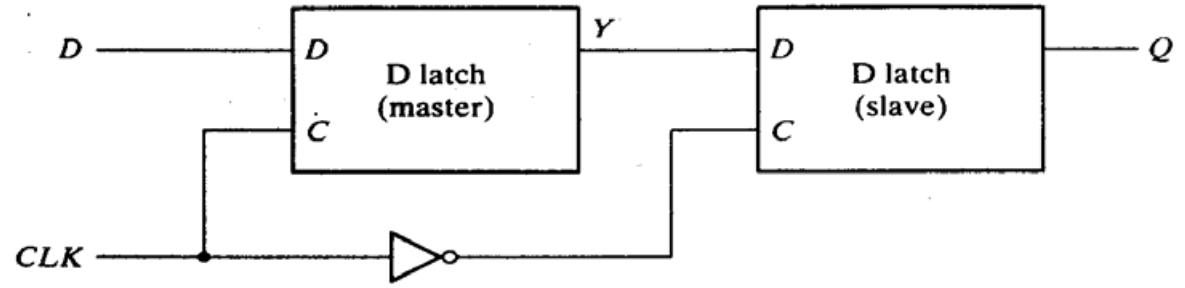


Figure 8 - D Flip Flop Using D Latches

D	Q(t+1)
0	0 RESET
1	1 SET

Table 1 - D Flip Flop Truth Table

T Flip Flop

T flip flop is also known as "Toggle Flip – flop". Toggle is to change the output to complement of the previous state in the presence of clock input signal.[7]

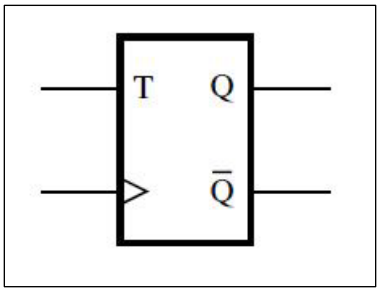


Figure 9 - T Flip Flop Block Diagram

T flip flop can be designed using a D flip flop and an xor gate as follows:

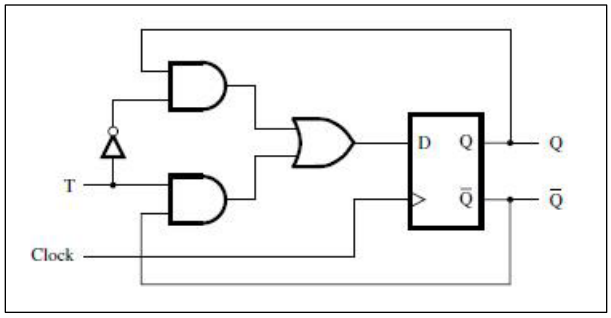


Figure 10 - T Flip Flop Logic Diagra

JK Flip Flop

JK flip – flop is named after the electrical engineer Jack Kilby."8 "The JK flip-flop is versatile. It can be used to store data, just like the D flip-flop. It can also be used to build counters, because it behaves like the T flip-flop if its J and K input terminals are connected together.[9]

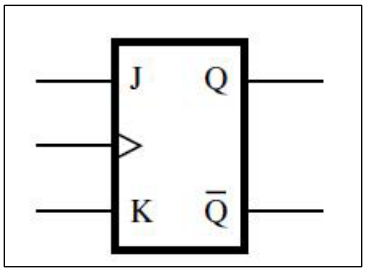


Figure 11 - JK Flip Flop Block Diagram

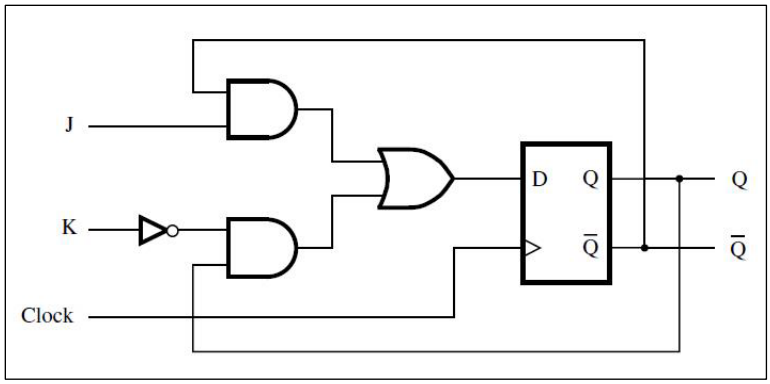


Figure 12 - JK Flip Flop Logic Diagram

REGISTERS

An individual flip-flop can be used to store one bit. However, in machines in which data are handled in words consisting of many bits (perhaps as many as 64), it is convenient to arrange a number of flip-flops into a common structure called a register. The operation of all flip-flops in a register is synchronized by a common clock. Thus, data are written (loaded) into or read from all flip-flops at the same time.[10]

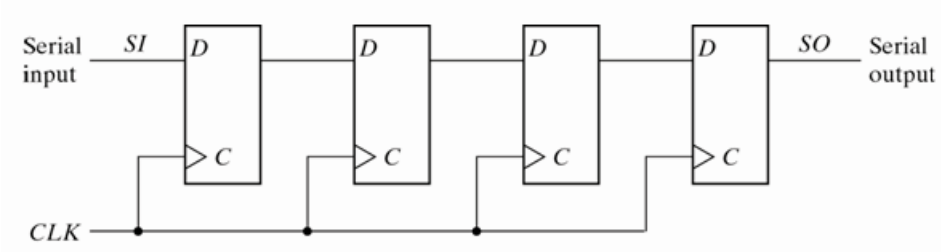


Figure 13: 4-bit Register

Shift register is a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Figure 14 shows 4-bit shift- right register.

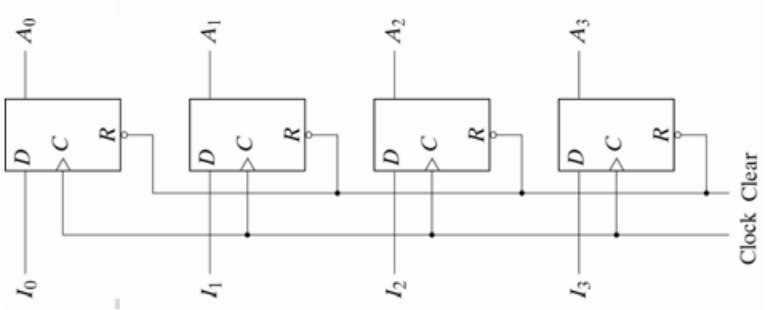


Figure 14: 4-bit shift- right register

COUNTERS

A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random. The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follows the binary number sequence is called a binary counter. An n -bit binary counter consists of n flip-flops and can count in binary from 0 through 2n - 1.[13]

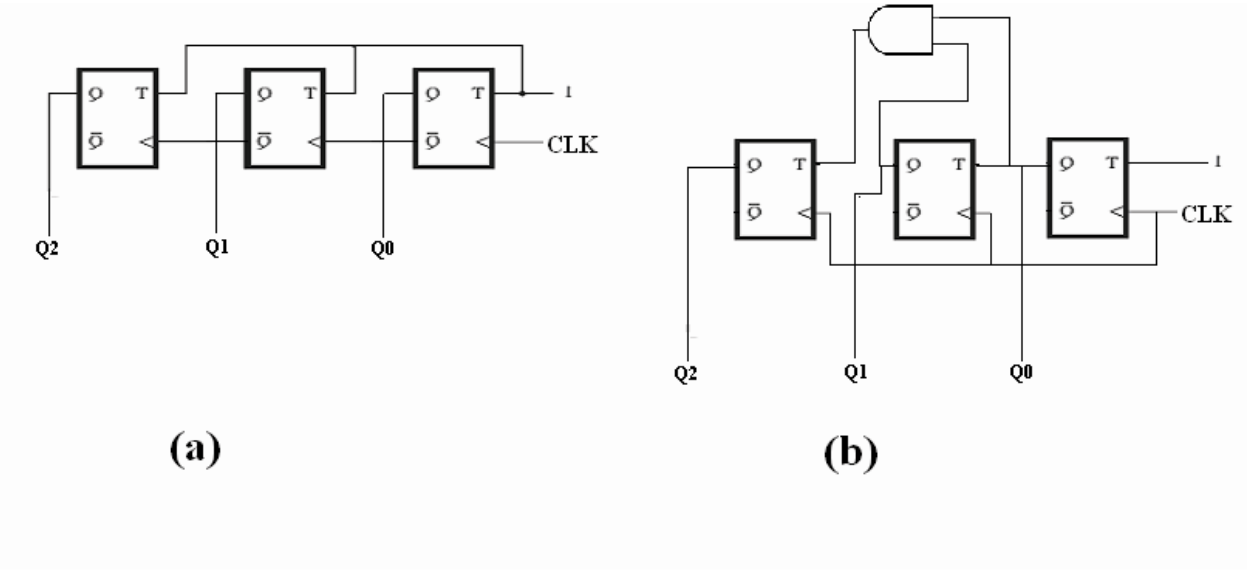


Figure 15: (a) 3-bit ripple counters, (b) 3-bit synchronous counter

Procedure and Discussion

LATCHES AND FLIP FLOPS

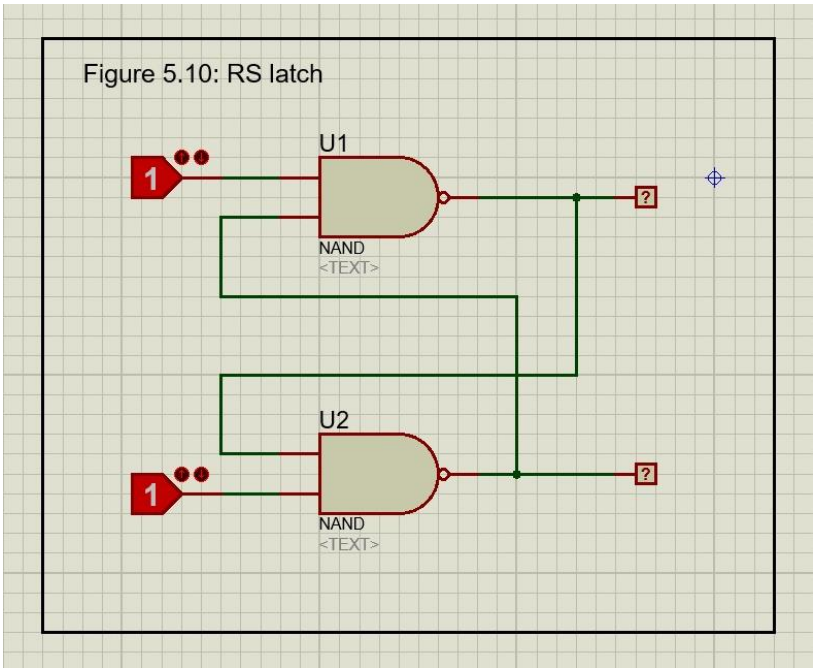


Figure 16: RS Latch

The RS latch results are active low, so when set and reset are 0 the latch doesn't have a determinate value so it gives error value that's unstable.

S	R	Q	Q'
0	**0**	ERROR VALUE	
0	**1**	1	0
1	**0**	0	1
1	**1**	NO CHANGE	

Table 2 -RS Latch

The gated RS latch results here are active high.

S	R	Q	Q'
0	**0**	ERROR VALUE	
0	**1**	1	0
1	**0**	0	1
1	**1**	NO CHANGE	

Table 3 - Gated RS Latch

Constructing RS latch with control input :

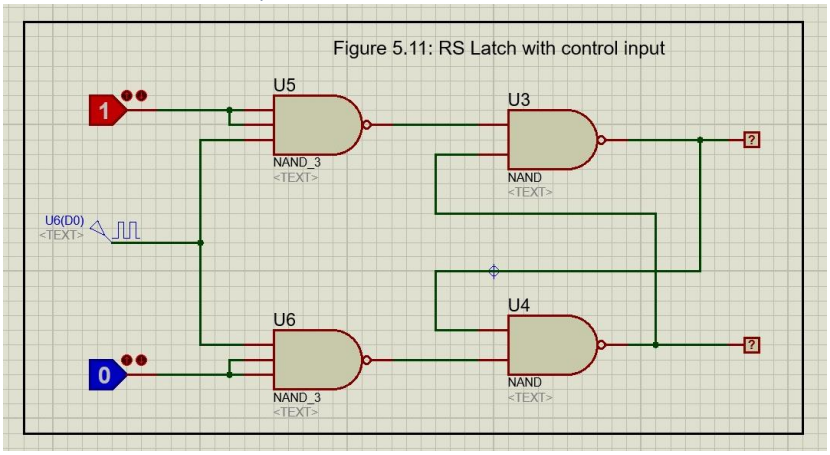


Figure 17: RS Latch with control input

A3(R)		A4(S)	CK2 =0		CK2=1
F6(Q)		F7(Q~)	F6(Q)		F7(Q~)
0	0	1	0	1	0
0	1	1	0	0	1
1	1	1	0	1	1
1	0	1	0	1	0
1	1	1	0	1	1
0	1	1	0	0	1
1	1	1	0	1	1

Table 4: RS latch with control input truth table

We can see that when the control CK2 = 0 the output won't change (CK2 works as an enable). When CK2 =1 the output will depend on values of RS as explained in the previous section *

Constructing D-latch with RS latch :

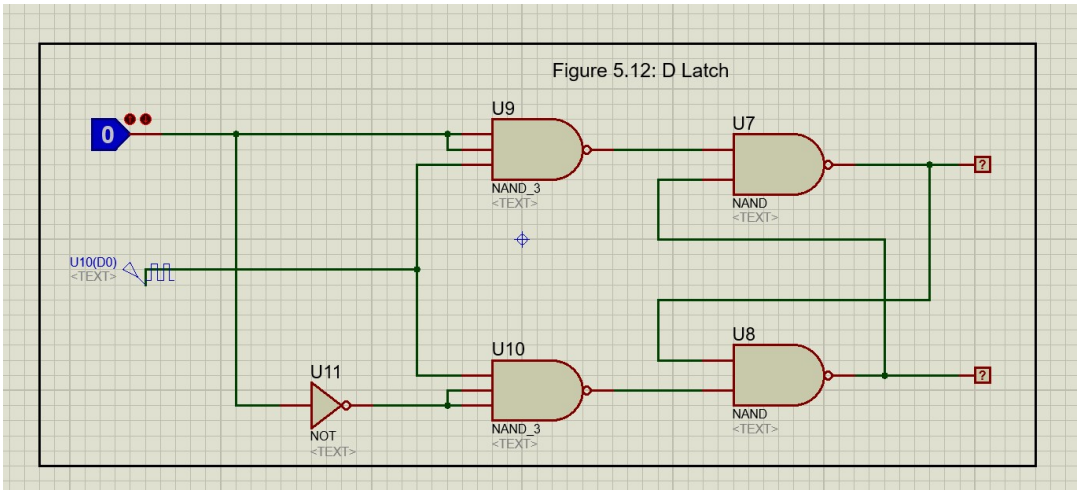


Figure 18: D-Latch

CK(En)	A1(D)	F6(Q)
0	0	1
0	1	1
1	0	0
1	1	1

Table 5: D latch truth table

Constructing JK latch with RS latch

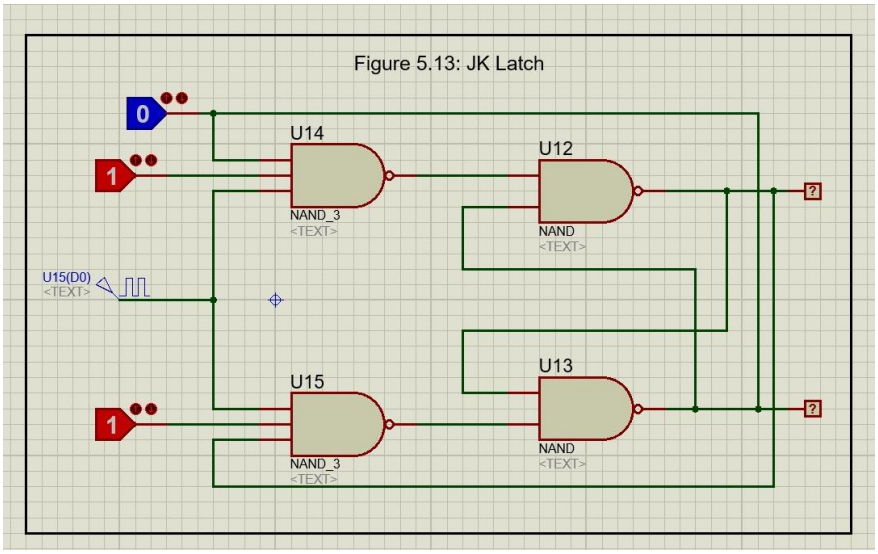


Figure 19: JK Latch

CK2(En)	A1(J)	A5(K)	F6(Q)
1	0	0	1
1	0	1	0
1	1	1	1
1	1	0	1
1	1	1	1
1	0	1	0
1	1	1	1

Table 6: JK Latch Truth Table

Constructing JK Flip-flop with master- slave RS latches

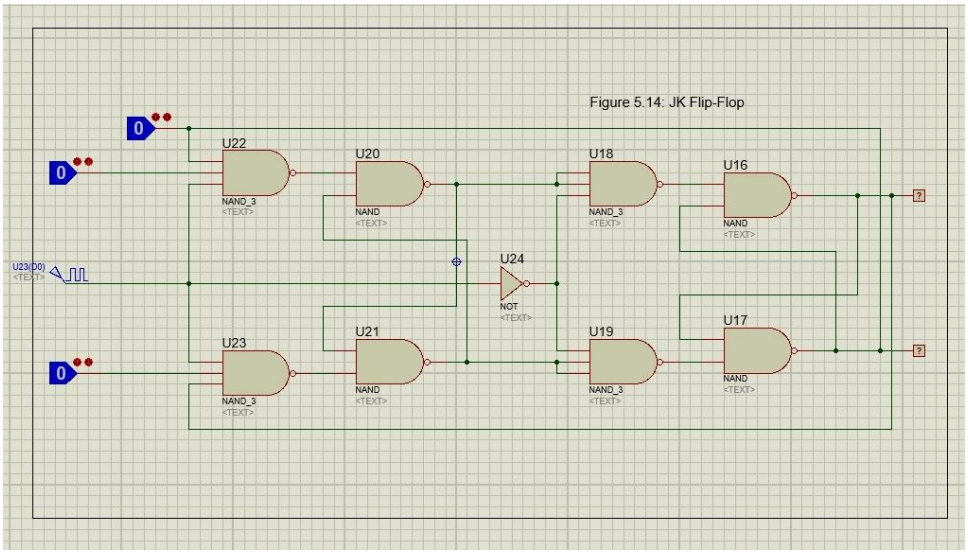


Figure 20: JK Flip-Flop

CK	J	K	F1(S)	F2(R)	F6(Q)	F7(Q~)
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	1	1	0	0	1
1	1	0	1	0	0	1
1	1	1	1	0	0	1
1	0	1	1	0	0	1
1	1	1	1	0	0	1

Table 7: JK flip flop with master slave RS latch truth table.

Registers

Constructing Shift Register with D Flip-Flops

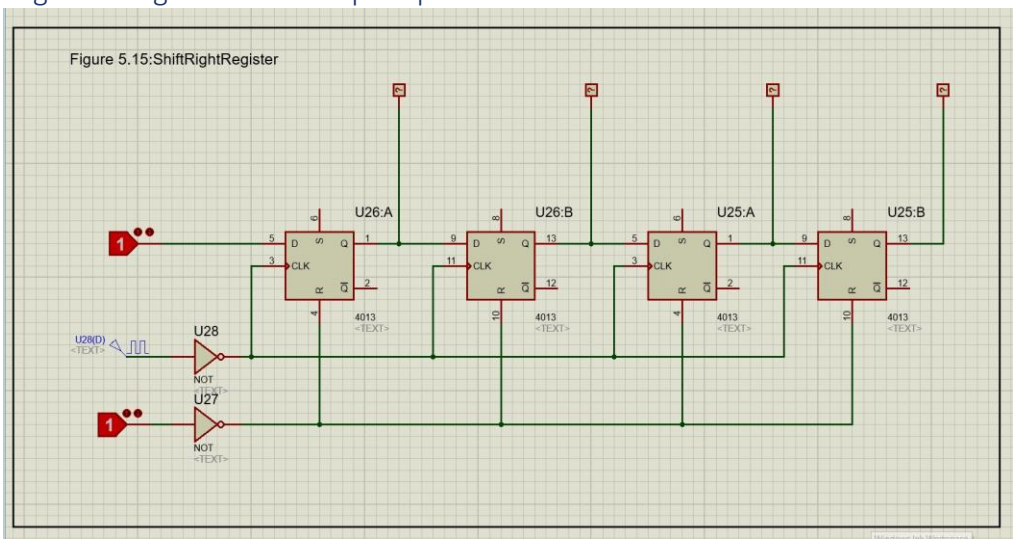


Figure 21: ShiftRightRegister

CK	B	A	F1	F2	F3	F4
1	0	x	0	0	0	0
1	1	1	1	0	0	0
1	1	0	0	1	0	0
1	1	0	0	0	1	0
1	1	1	1	0	0	1

Table 8: Shift register with D flip-flop truth table .

4-Bit Shift Register withserial and parallel load

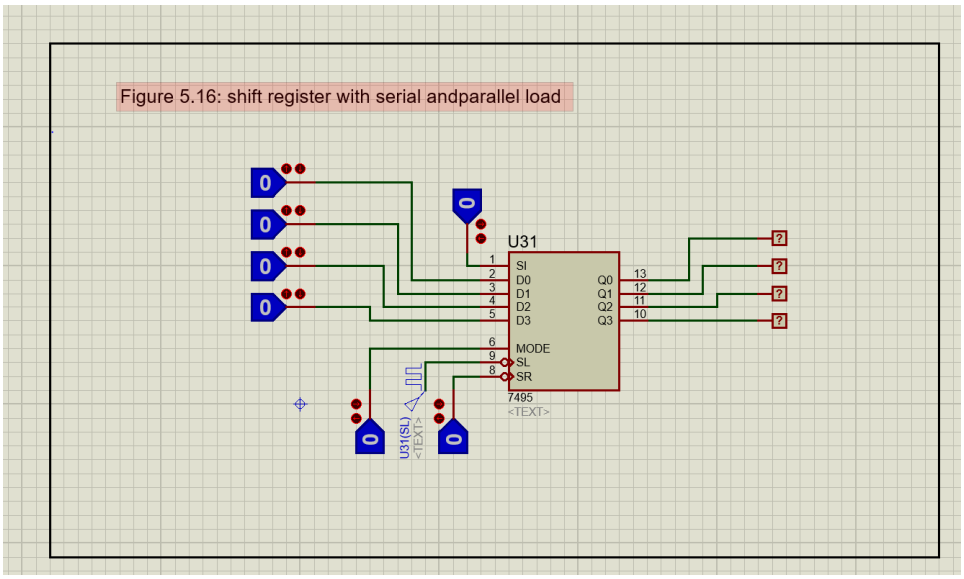


Figure 22: shift register with serial andparallel load

INPUTS			OUTPUTS		
CK	A1	L3	L2	L1	L0
1	0	0	1	1	1
1	0	0	0	1	1
1	0	0	0	0	1
1	1	1	0	0	0

Table 9: 4-bit shift register truth table .

INPUTS					OUTPUTS			
D1	D	C	B	A	L3	L2	L1	L0
1	0	0	1	0	0	0	1	0
1	1	0	1	0	1	0	1	0
1	1	1	1	0	1	1	1	0
1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	0

Table 10: Table shows the measured results after following the given input sequence

Counters

2-bit Synchronous Counter

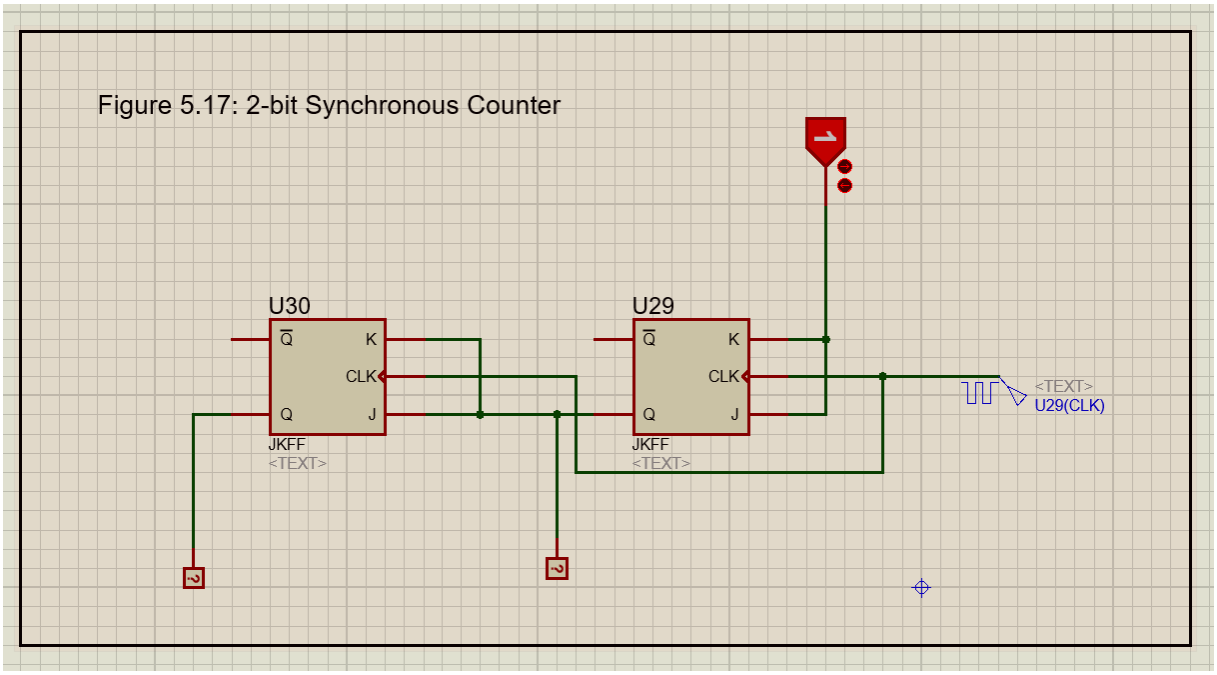


Figure 23: 2-bit synchronous counter

INPUT	OUTPUTS	
CLK	Q1	Q2
1	0	0
1	0	1
1	1	0
1	1	1
1	0	0
1	0	1

Table 11: 2-bit synchronous counter truth table .

3-bit (divide-by-eight) Ripple Counter

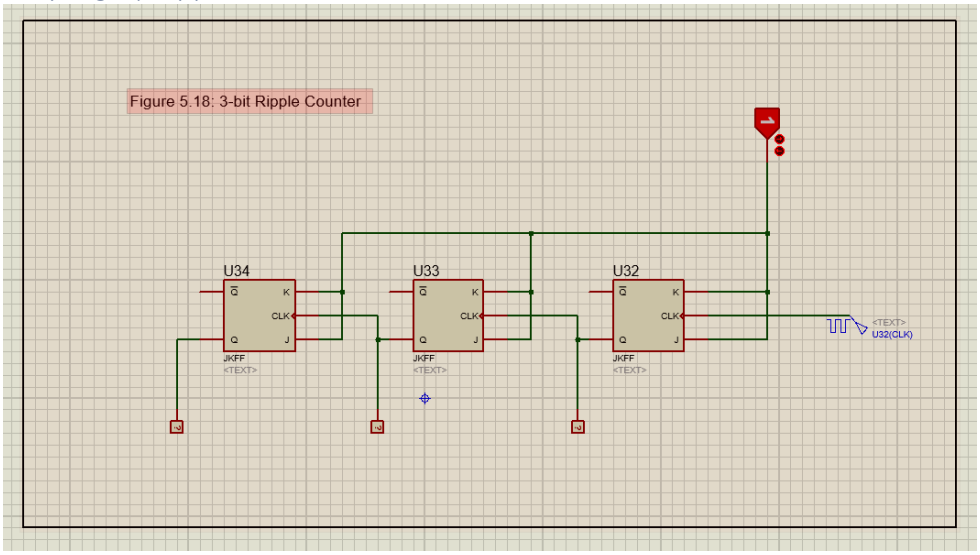


Figure 24: 3-bit Ripple Counter

INPUT	OUTPUTS		
CLK	Q2	Q1	Q0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
1	0	0	0

INPUT	OUTPUT
CLK	D
1	0
1	1
1	2
1	3
1	4
1	5
1	6
1	7
1	0

Table 12: 3-bit Ripple counter Truth Table

BCD Counter

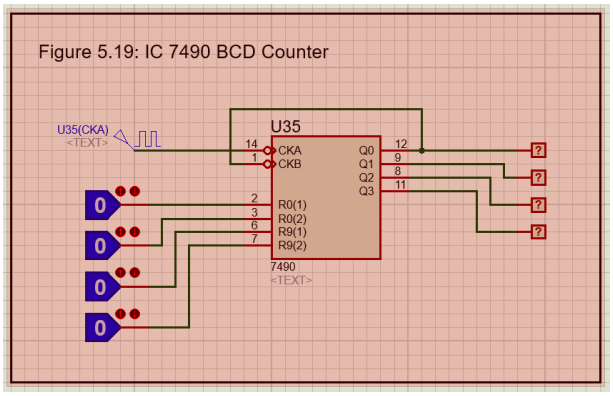


Figure 25: IC 7490 BCD Counter

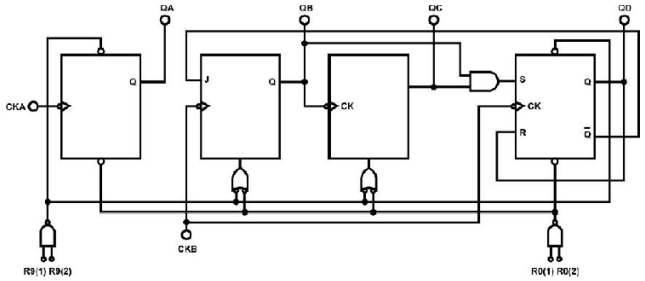


Figure 26: IC 7490 BCD Counter

INPUTS			OUTPUTS		
A	**B**	**F4**	**F3**	**F2**	**F1**
1	1	0	0	0	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	0	1
1	1	0	0	0	0

Table 13: BCD counter (0-9)

Divide-by-8 counter using BCD chip counter

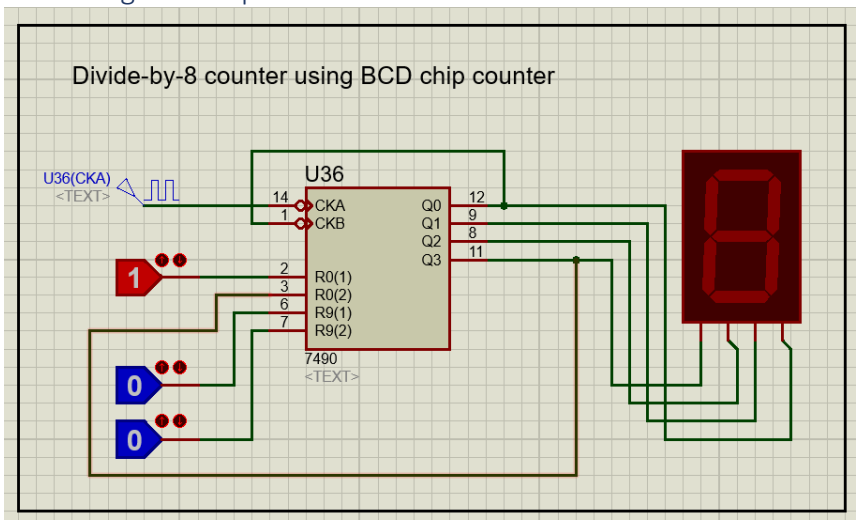


Figure 27: Divide-by-8 counter using BCD chip counter

INPUTS			OUTPUTS		
A	**B**	**F4**	**F3**	**F2**	**F1**
1	1	0	0	0	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	0	1	1	1
1	1	0	0	0	0

Table 14: Divide by 8 counter truth table

Divide by 6 counter

- The same connection in above were used .

- R0(1) was connected to QC .

- R0(2) was connected to QB .

- When QA , QB , QC , QD = 0110 , the counter resets (the shown output will be only 5).

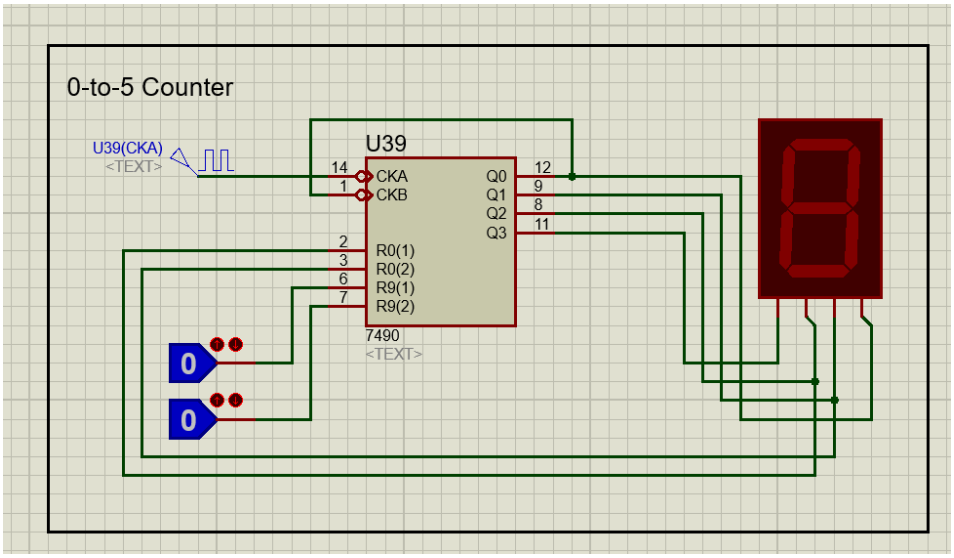


Figure 28: Divide-by-6 counter using BCD chip counter

Divide by 5 counter :

- The same connection in above were used .

- R0(1) was connected to QA .

- R0(2) was connected to QB .

- When QA , QB , QC , QD = 1010 , the counter resets (the shown output will be only 4) .

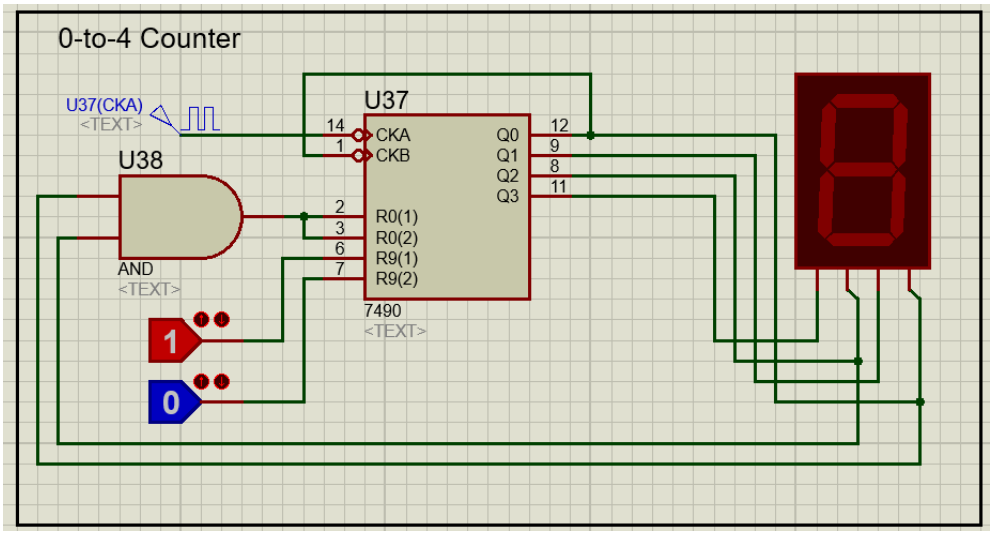


Figure 29: : Divide-by-5 counter using BCD chip counter

DISCUSSION

1. Because latches are triggered on levels (only work when CLK =1) . Sequential circuits are triggered on edge (positive edge or negative) .

2. The undefined output when RS =11

3. The ripple has different clocks , the synchronous has a common clock

Conclusion

Although RS latches do have a problem when it comes to the R=1, S=1 condition, but that doesn't mean that latches are not used. Latches are used with the 8088/8086 microprocessors to latch address lines going to the memory.

Latch is faster because it has no need to wait for a clock signal so they are most used in high speed designs and they require less power.[16]

Flip flops are widely used in the digital systems, SRAMs are expensive because they're fast and made of flipflops, nevertheless, they are used in counters – which are used for many applications such as frequency division, digital clocks, analog to digital converter, etc.… -, and registers – which are mainly used with processors to store temporary data fast.

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