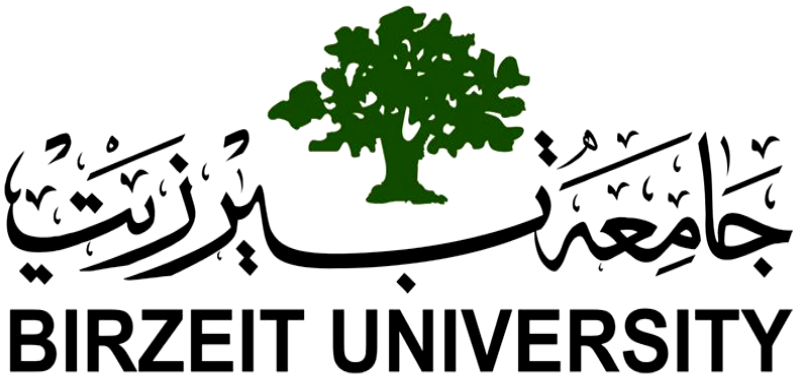

Faculty of Engineering & Technology
Electrical & Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY - ENCS2110

Report #4

Constructing Memory Circuits Using Flip-Flops

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Abstract

The aims of this experiment are to understand the basic structure of Random-Access Memory (RAM). And to understand and test the circuit of 64-bit Random Access Memory (RAM).

Contents

Theory

Random Access Memory is a type of data storage element that is used in every electronic device, it's faster than normal memory (ROM), used to store the operating system, applications and other temporary data. RAM is constructed sing flip-flops, and its capacity is determined by the number of address lines There are two different types of basic structure for RAM:

i. CONSTRUCTING RANDOM ACCESS MEMORY (RAM) WITH D FLIP-FLOP

The input and output are not separated shown in (fig 1a). There are two control terminals: one is the R/W terminal (R for READ or OUTPUT, W for WRITE or INPUT) and the other one is the ENABLE terminal. When CS=0, tri-state gates U1 and U2 do not operate, so data input is not possible, the flip-flop output Q is not sent to the I/O terminal. When CS=1, W/R controls the D flip-flop. When W/R' =1, U1 opens but U2 does not, I/O will accept data input. If W/R'=0, the exact opposite will happen and I/O act as the data output. The connection shown in (fig 1b) will increase the RAM capacity. When CS1=1, RAM1 I/O1 and I/O2 are selected. Address line A is used to select between RAM1 and RAM2. Since there is only one address line, we can only select from 2 RAMs. [1]

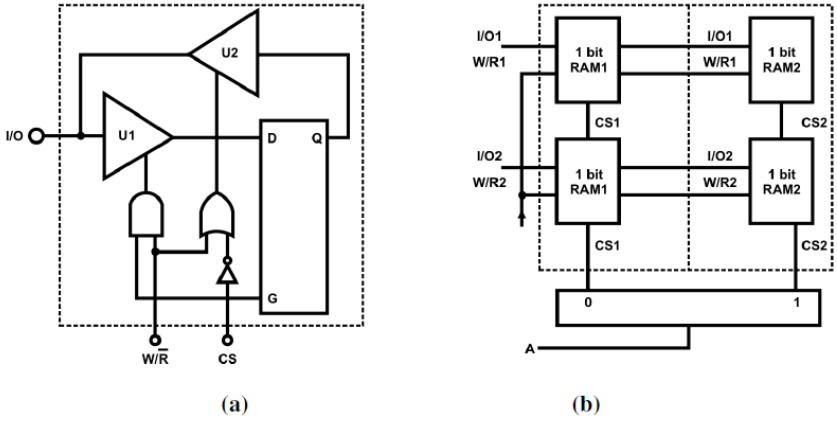


Figure 1

A 2-address (2-bit) RAM circuit has independent input and output shown I (fig 2). When Address=0, input D1 is enabled and the content of D1 will be made available at the output. When Address=1, input D2 is enabled and the content of D2 will be made available at the output. The ENABLE terminal must be triggered in order for the output to correspond with the constantly changing inputs.

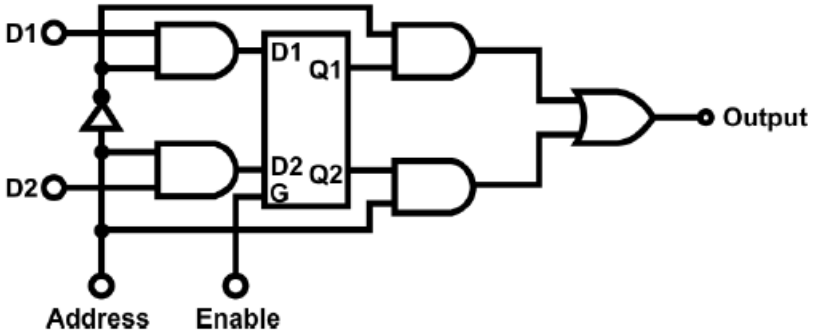


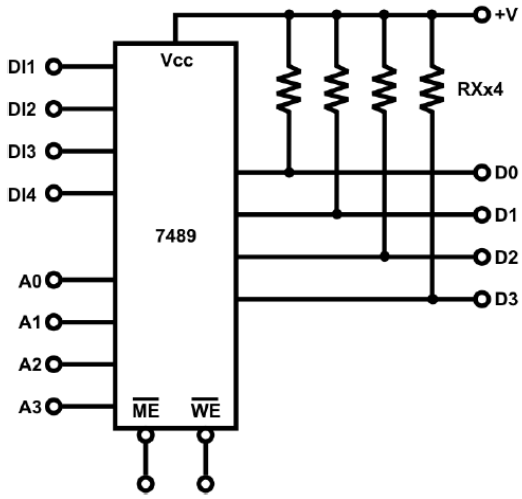
Figure 2

ii. 64-BIT RANDOM ACCESS MEMORY (RAM) CIRCUIT

To select between the data during the process the operation is controlled by address selectors. The length of data is related to the number of data variations. For example, if there are 4 data then 2^4 data variations exist.

The number of locations that can be addressed is determined by the number of address lines, if there are 4 address lines, then 2^4locations exist.

A 4-bit data can be stored in each location, since the total capacity is 16×4, where the 4 is the number of data while 16 is the number of address lines. Fig3 shows a 16×4 memory with 64 memory capacity.



$\overline{ME}$	$\overline{WE}$	
0	0	Write
0	1	Read
1	0	Inhibit storage
1	1	Do nothing

Figure 3

When ME' = 0 and WE' = 0, the memory is enabled and the input process starts. The input and output terminals are separated. The output terminals are open-collector type so resistors "RX×4" must be added to the supply voltage.

Since the output terminal of 7489 is open-collector type, the outputs can be connected in parallel, as shown in Fig.4. The operating sequence will be controlled by ME' and WE'.

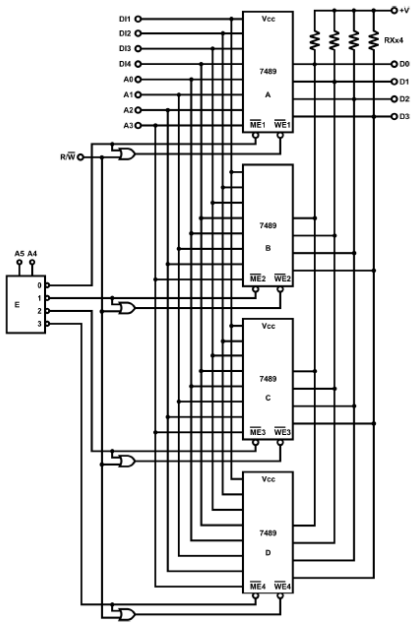


Figure 4

When A4A5=00, A is selected, ME' and WE' of B, C and D all equal to “1”. Similarly, when A4A5=01, B is selected, ME' and WE' of C and D all equal to “1”. E is 2-4 decoders with “0” as its output. The unselected outputs are in high or “1” state.

Since the outputs will have high impedance when ME' and WE' are both “1”, each R/W' control of 7489 are connected to an OR gate to ensure that when ME' = “1”, WE' will be equal to “1” too.

When ME' = “0”, WE' is controlled by external R/W' control so that the “READ” operation is performed if R/W'= “1”. The “WRITE” operation is performed when R/W'= “0”.

The 7488 is a 256-bit open-collector ROM which has similar structure as the 7489. Their methods of expansion are similar as well.[2]

Procedure

The logic diagram was designed using Protues software as follow:

i. 2-bit Random Access Memory (RAM) with D Flip-Flop:

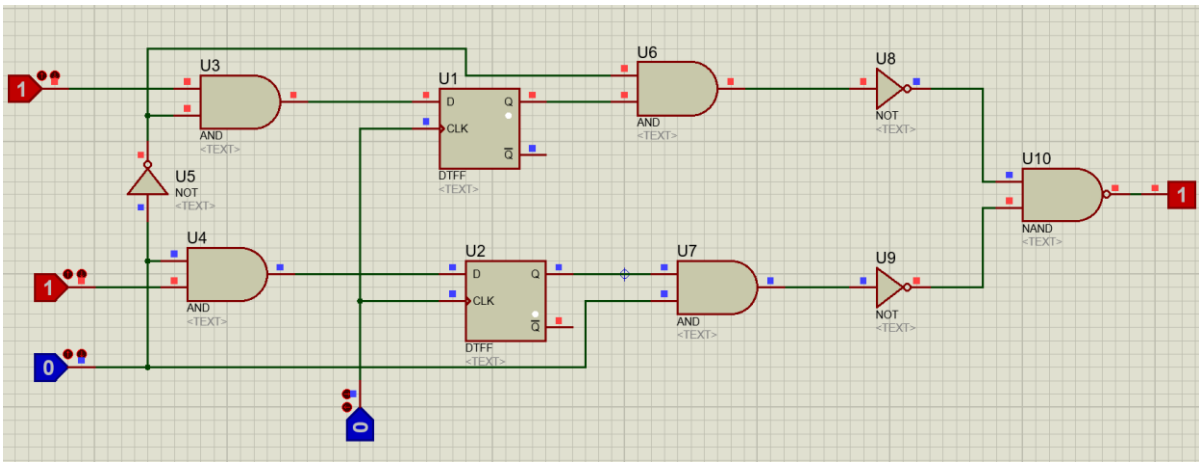


Figure 5: 2-bit RAM with D Flip-Flop

Table 1: : 2-bit RAM with D Flip-Flop Truth Table

input				Output		
E1	S1	D1	D2	F3	F2	F1
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	0
1	1	1	1	1	1	0

ii. 8-bit Random Access Memory (RAM) with D Flip-Flop:

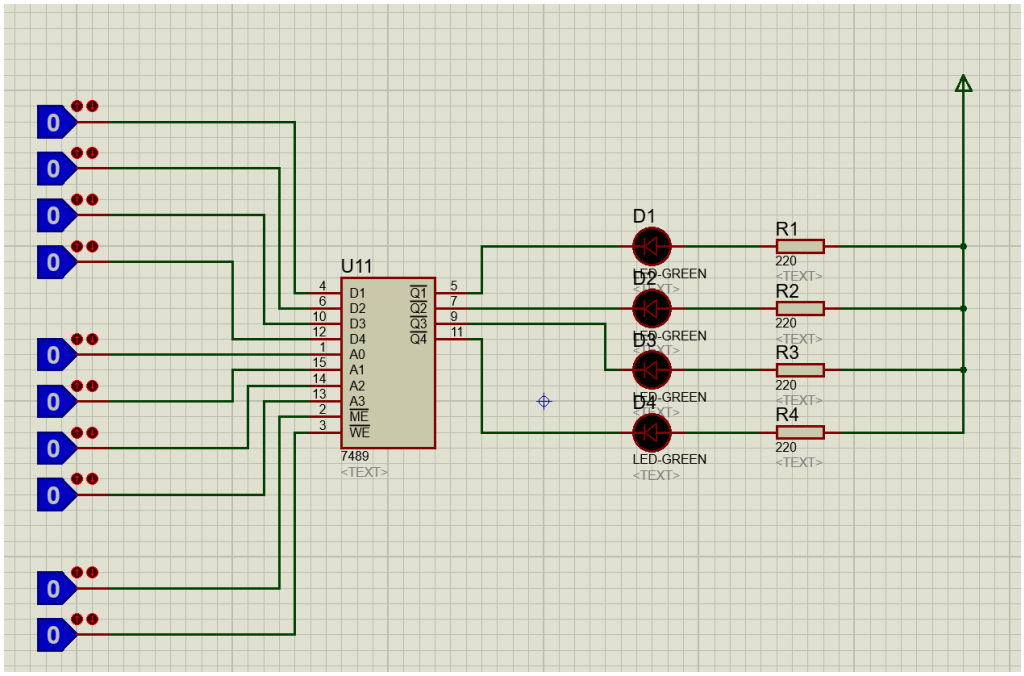


Figure 6: 8-bit RAM with D Flip-Flop

iii. 64-BIT RANDOM ACCESS MEMORY (RAM) CIRCUIT

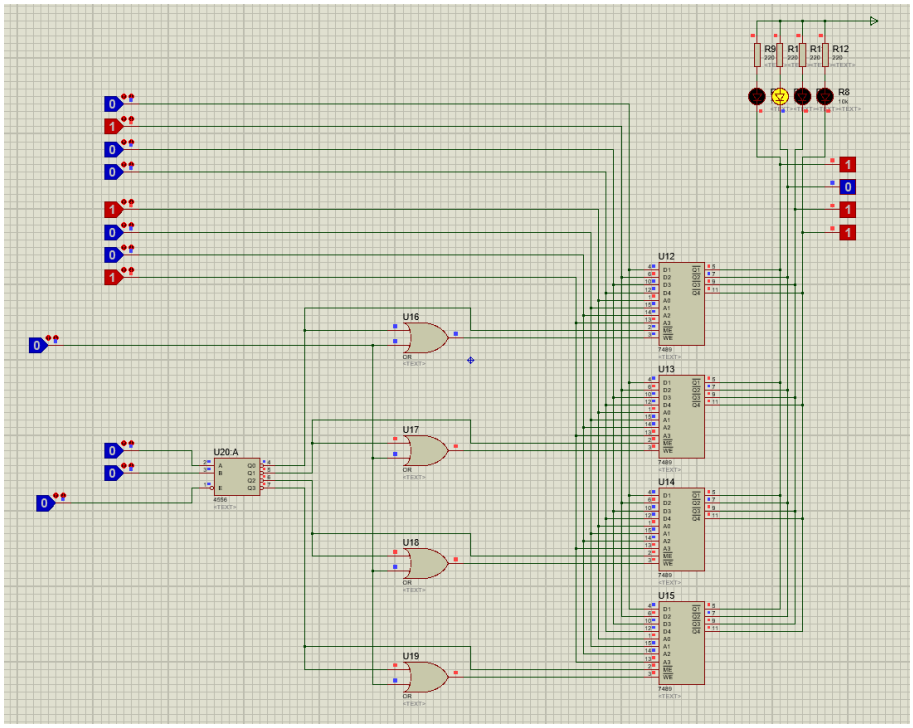


Figure 7: 64-bit RAM CIRCUIT

Conclusion

To wrap it all we can say that a storage element can be implemented in different ways, and could have various capacities depending on the number of address lines. Data is stored in certain locations in the memory and can be accessed only by these addresses. The RAM memory is a volatile storage element that doesn't keep the data after removing the power supply and is used for storing the operating system, applications and other data temporary.

References

[1][2] ENCS211 Lab Manual. Accessed on 13/10/2020 at 10:31AM.