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Ex.8 ToDo

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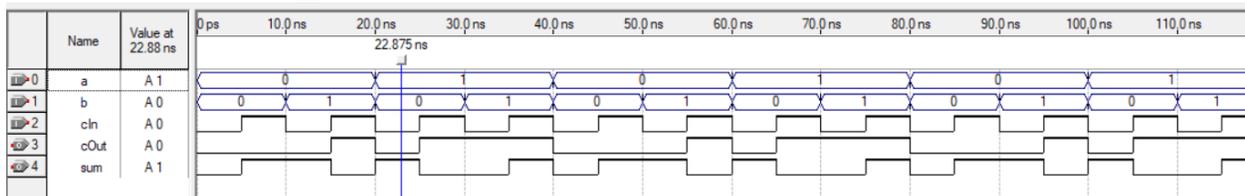
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fullAdder

code

```
1 module fullAdder(a, b, cIn, sum, cOut);
2
3     input a, b, cIn;
4     output reg sum, cOut;
5
6
7     always @(a, b, cIn)
8     begin
9         {cOut, sum} = a + b + cIn;
10    end
11
12 endmodule
```

Simulation

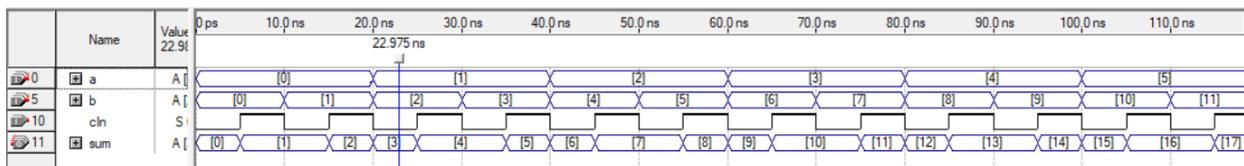


fourBitFullAdder

code

```
1 module fourBitFullAdder(a, b, cIn, sum);
2
3     input [3:0] a, b;
4     input cIn;
5     output [4:0] sum;
6
7     wire w1, w2, w3;
8
9     fullAdder f1(a[0], b[0], cIn, sum[0], w1);
10    fullAdder f2(a[1], b[1], w1, sum[1], w2);
11    fullAdder f3(a[2], b[2], w2, sum[2], w3);
12    fullAdder f4(a[3], b[3], w3, sum[3], sum[4]);
13
14 endmodule
```

Simulation

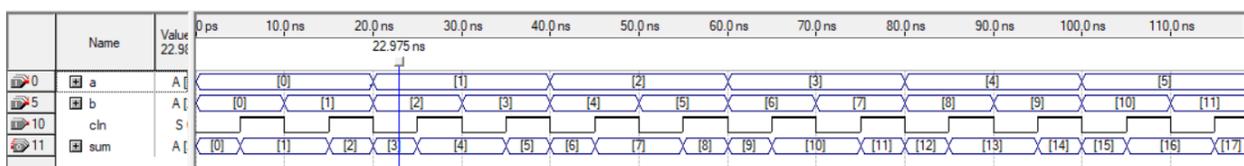


fourBitComparator

code

```
1  module fourBitComparator(a, b, result);
2
3      input [3:0] a, b;
4      output reg [2:0] result;
5
6      always @(a, b)
7      begin
8
9          if(a>b)
10         begin
11             result = 3'b100;
12         end
13
14
15         else if(a==b)
16         begin
17             result = 3'b010;
18         end
19
20
21         else if(a<b)
22         begin
23             result = 3'b001;
24         end
25
26     end
27 endmodule
```

Simulation

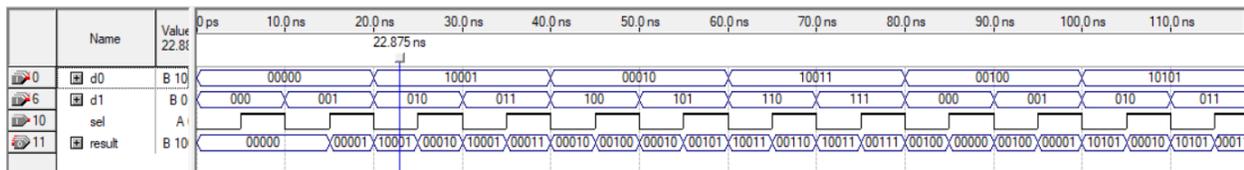


twoByOneMux

code

```
1 module twoByOneMux(d0, d1, sel, result);
2
3     input [4:0] d0;
4     input [2:0] d1;
5     input sel;
6     output reg [4:0] result;
7
8     always @(d0, d1)
9     begin
10
11         if(sel)
12             result = d1;
13
14         else
15             result = d0;
16
17     end
18
19 endmodule
20
```

Simulation



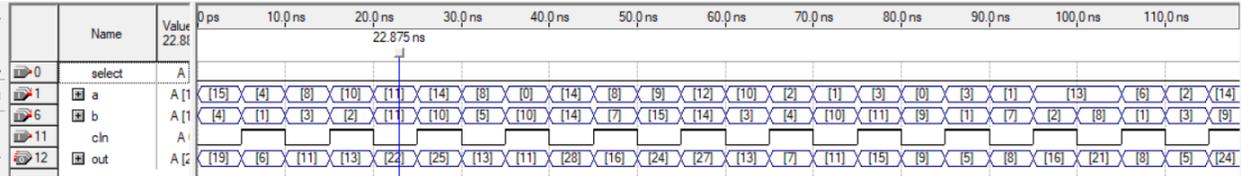
project

code

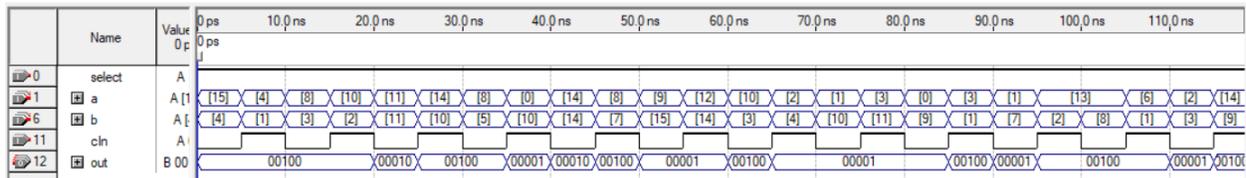
```
1 module project(a, b, cIn, select, out);
2
3     input [3:0] a, b;
4     input cIn, select;
5     output [4:0] out;
6
7     wire [4:0] w1;
8     wire [2:0] w2;
9
10
11     fourBitFullAdder(a, b, cIn, w1);
12     fourBitComparator(a, b, w2);
13
14     twoByOneMux(w1, w2, select, out);
15
16 endmodule |
```

Simulation

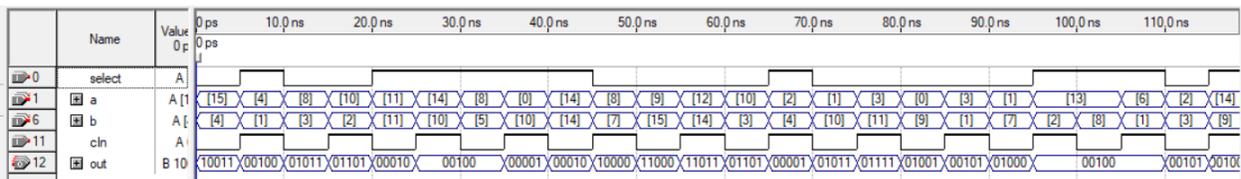
Select=0 (adding)



Select=1 (comparing)



Both selections (Randomly)



Schematic

