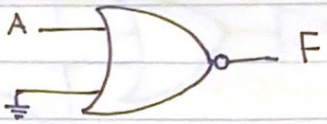
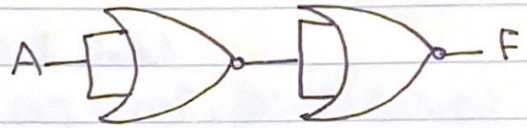
exp. 1

1- NOR Gate Circuit

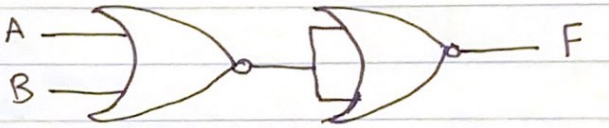
- NOR as NOT



- NOR as a Buffer

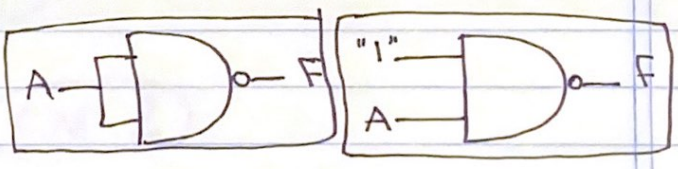


- NOR as OR

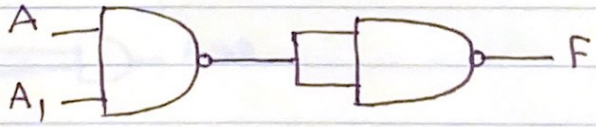


2- NAND Gate Circuit

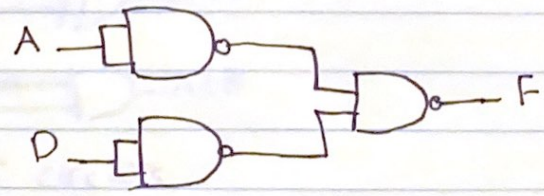
- NAND as NOT



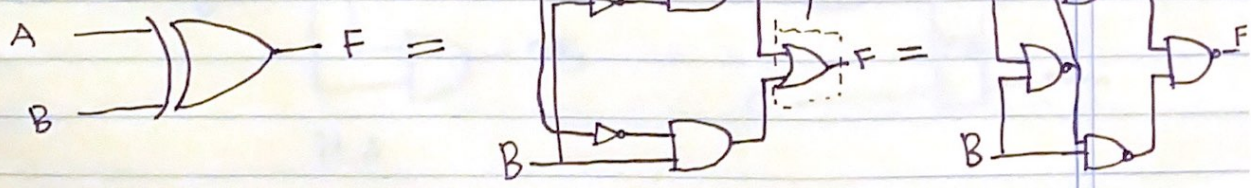
- NAND as AND



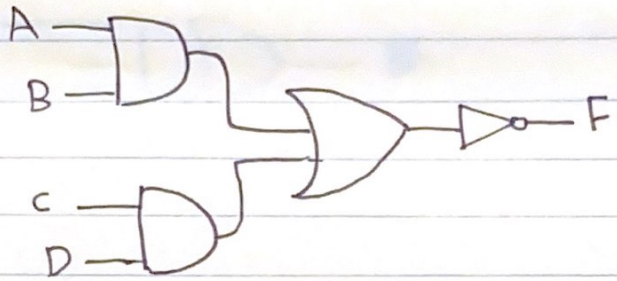
- NAND as OR



3- XOR Gate Circuit

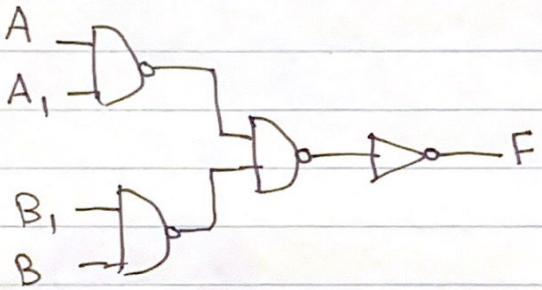


4- AOI (AND-OR-INVERTER) Gate circuit



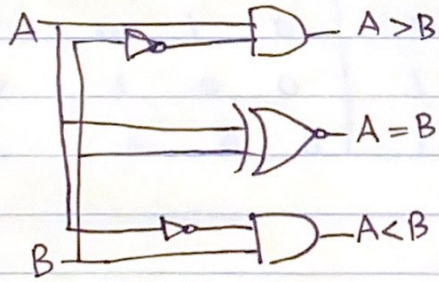
(AOI Gate)

$F = (AB + CD)' = (A'+B')(C'+D')$

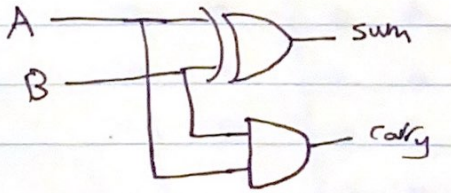


exp. 2

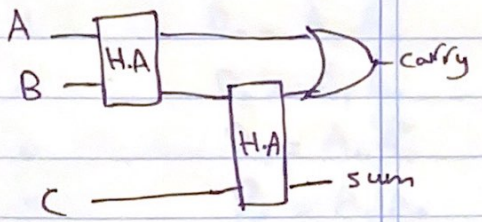
1- Comparator circuit



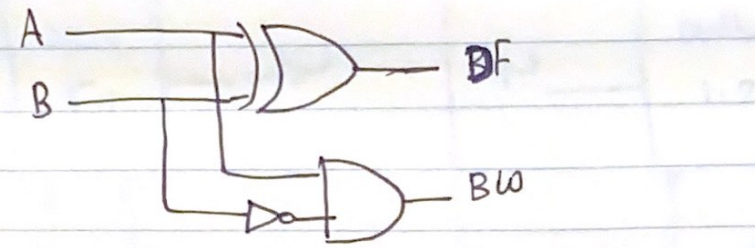
2- Half- and Full- Adder circuits



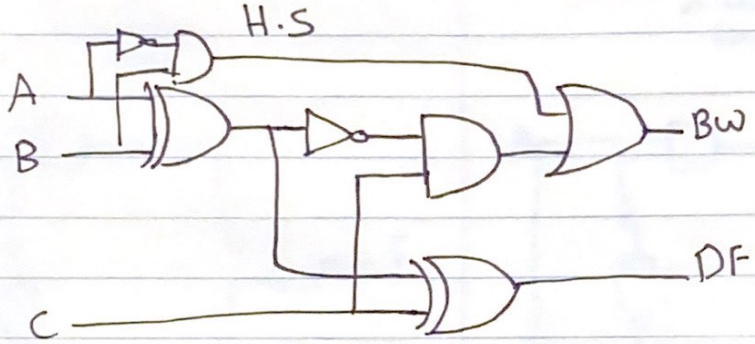
H.A



3- Half- And Full- subtractor



H.S

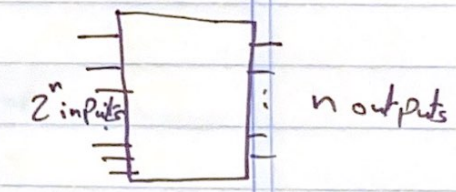


F.S

exp. 3

1- Encoder

A_3	A_2	A_1	A_0	D_1	D_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



2- Decoder

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

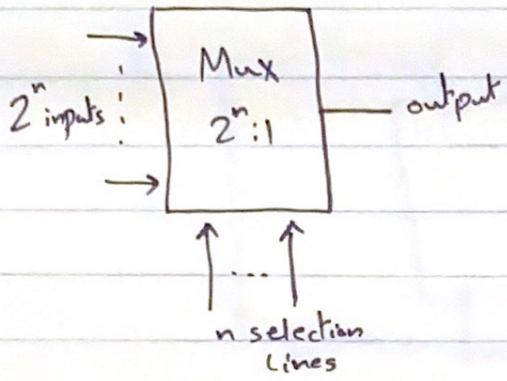
$D_0 = \bar{A}_1 . \bar{A}_0$

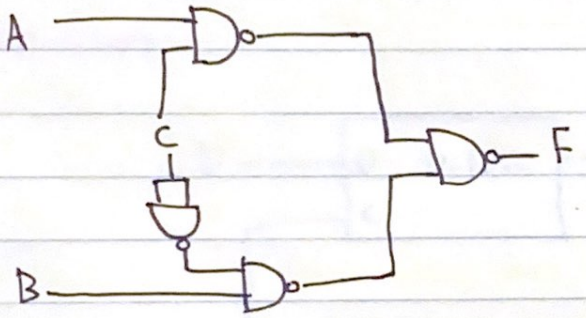
$D_1 = \bar{A}_1 . A_0$

$D_2 = A_1 . \bar{A}_0$

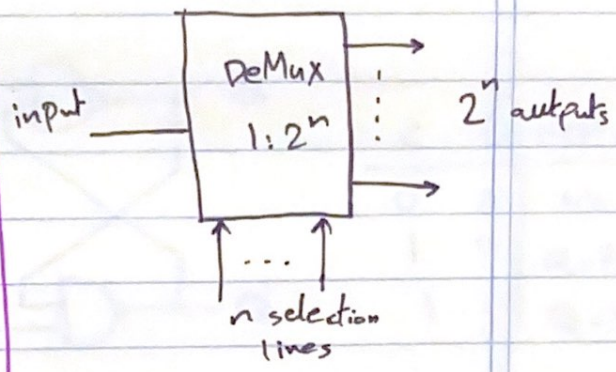
$D_3 = A_1 . A_0$

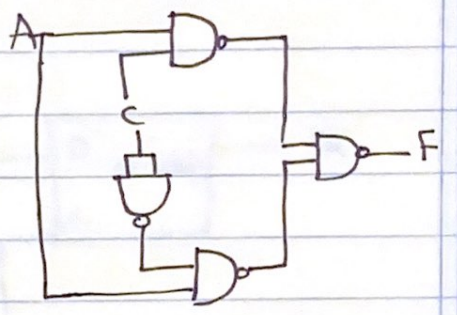
3- Multiplexer





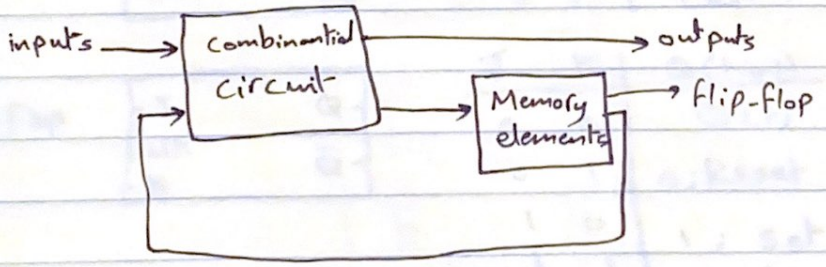
4- De Multiplexer





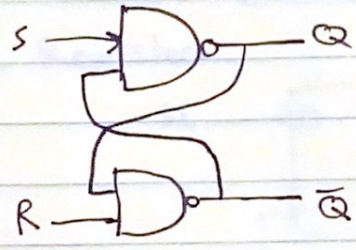
exp. 5

1- Sequential Circuits



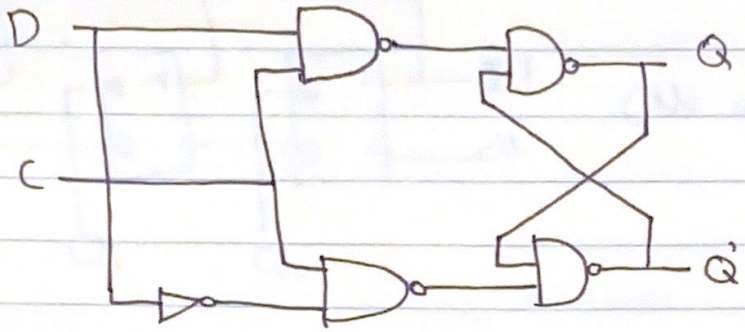
2- Latches

a. SR Latch



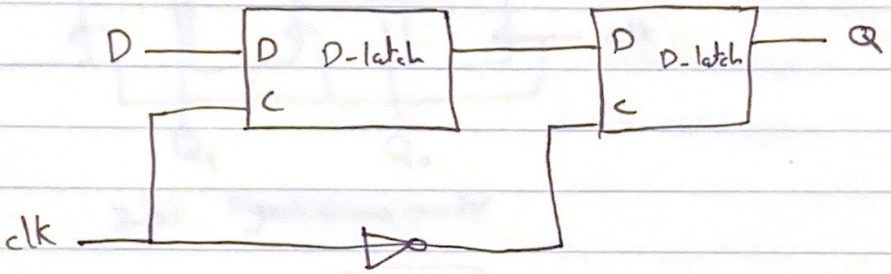
S	R	Q	$\dot{Q}$	
1	0	0	1	(Reset)
1	1	No change		
0	1	1	0	(set)
0	0	1	1	

b- The D Latch

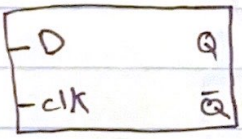


C	D	Next state Q
0	X	No change
1	0	Q = D; Reset
1	1	Q = 1; set

3- Flip-flops

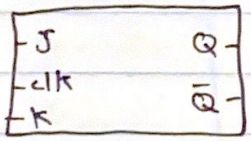


D-Flip-Flop



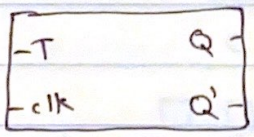
D	Q(t+1)
0	0 (Reset)
1	1 (set)

JK-Flip-Flop



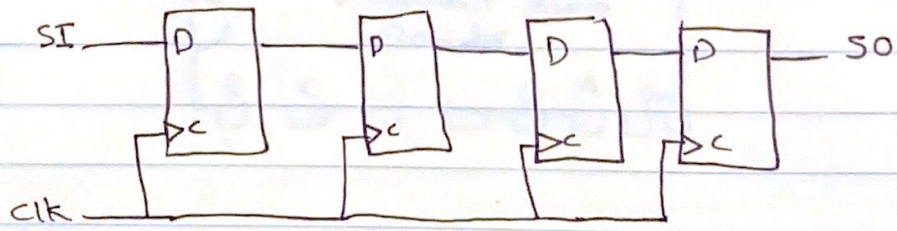
J	K	Q(t+1)
0	0	Q(t) ; No change
0	1	0; Reset
1	0	1 ; set
1	1	Q'(t) ; Complement

T-Flip-Flop

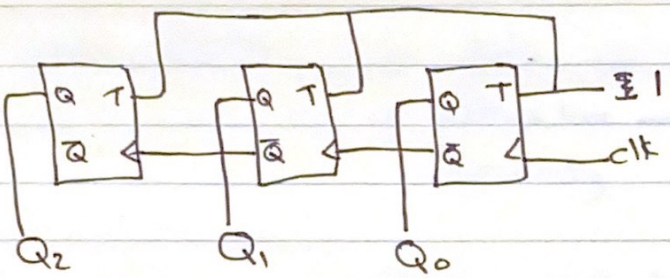


T	Q(t+1)
0	Q(t); No change
1	Q'(t); complement

4- Registers

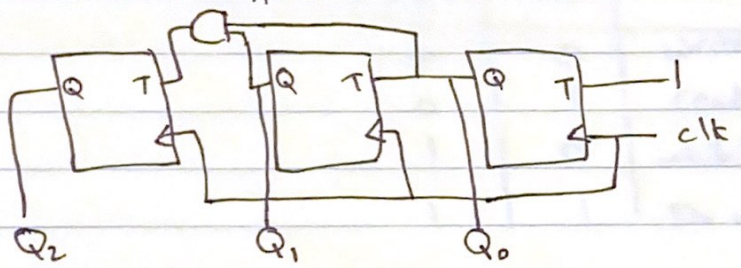


5 - Counters



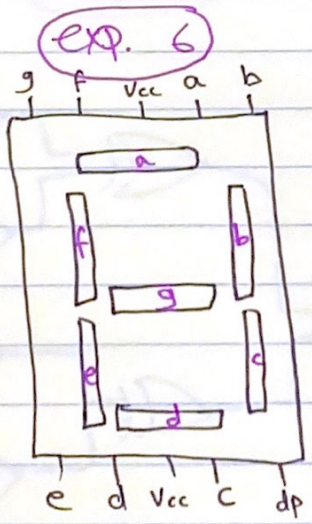
(No common clock)

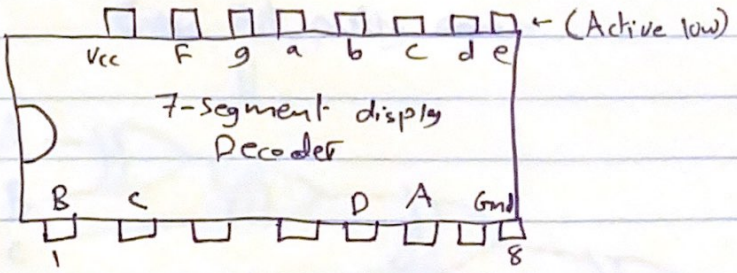
3-bit-ripple-counter



3-bit synchronous counter

exp. 6





← (Active low)

exp. 7

*In RAM: n data → 2^n data variations

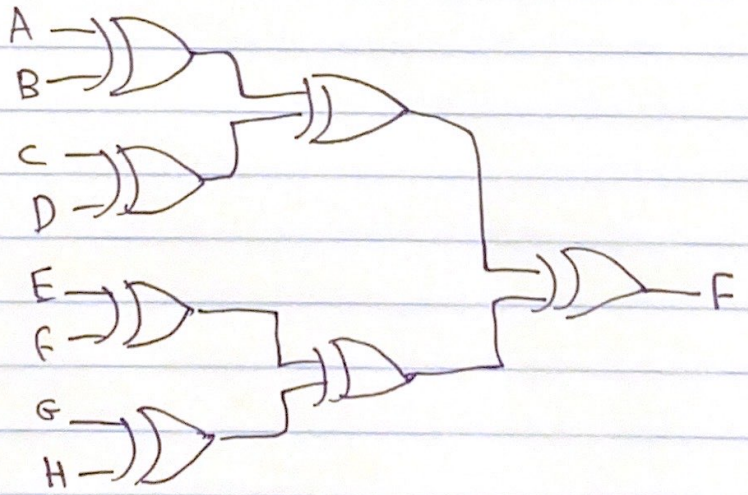
n address line → 2^n locations

capacity : locations X number of bits

16 x 4 memory truth table

$\overline{ME}$	$\overline{WE}$	
0	0	write
0	1	read
1	0	inhibit storage
1	1	Do nothing

exp. 11



Even Bit parity Gene...