BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Electrical and Computer Engineering Department

ENCS2340 Digital Systems

First Semester 2022/2023

Course Catalog

3 Credit hours (3 h lectures).

Number Systems. Boolean Algebra. Logic Gates. Simplification of Boolean functions. Design of Combinational Logic. Sequential Logic: latches, flip-flops, state diagrams and excitation tables. Registers, counters, and sequential systems, derivation of state tables and state diagrams. Memory units. Introduction to Programmable Logic Devices, and Hardware Description Languages.

Text Book(s)

Title	Digital Design
Author(s)	M. Morris Mano and Michael D. Ciletti
Publisher	Prentice Hall
Year	2012
Edition	5th Edition

References

Books	1. Fundamentals of Logic Design, Charles Roth, Jr., Brooks Cole. 7th Edition, 2013 2. Digital Design: Principles and Practices, John F. Wakerly, 4th Edition, Prentice Hall.2005

Instructors

Instructors	Dr. Ismail Khater (**Course Coordinator**) Dr. Mohammed Hussein Dr. Bilal Karaki Mrs. Anjad Badran Dr. Ibrahim Nemer Dr. Ali Abdo
Office Location- Coordinator	Masri515
E-mail-Coordinator	ikhater@birzeit.edu

Class Schedule & Rooms

	Class Number	Instructor Name	Number of Students / Capacity	Classes Time		
Lecture	1	Ismail Mohammad Mousa Khater	47 / 45	T, R	12:50 - 14:05	Masri204
Lecture	2	Ismail Mohammad Mousa Khater	45 / 45	M, W	11:25 - 12:40	Masri306
Lecture	3	Mohammed Sami Abdul Karim Hussein	45 / 45	S, M	11:25 - 12:40	Masri302
Lecture	4	Bilal Jafar Hamed Karaki	45 / 45	M, W	08:30 - 09:45	Masri306
Lecture	5	Anjad Jamal Rushdi Badran	48 / 45	T, R	10:00 - 11:15	Masri406
Lecture	6	Ibrahim Ahmed Abdallah Nemer	46 / 45	M W	12:50 - 14:05 12:50 - 14:05	Masri306 Masri406
Lecture	7	Ali Hasan Moath Abdo	33 / 45	S, M	08:00 - 09:15	Masri504
Lecture	8	Anjad Jamal Rushdi Badran	51 / 45	T, R	12:50 - 14:05	Bamieh205

Office Hours

Check **Ritaj** for the office hours of your Instructors

Prerequisites

Prerequisites by course	COMP230 or COMP132 or COMP142

Topics Covered

Topics	**Chapters in Text**	**Week number**
Binary Systems	Chapter 1	1
Boolean Algebra and Logic Gates	Chapter 2	2 – 3
Gate-Level Minimization	Chapter 3	4 – 5
Combinational Logic	Chapter 4	6 – 8
HDL for combinational logic		9
Midterm Exam		
Synchronous Sequential Logic	Chapter 5	10 – 12
Registers and Counters	Chapter 6	13-14
HDL for Sequential Logic		15

Error Correction and programmable logic.	Chapter 7	16

Mapping of Course Objectives to Program Outcomes	Assessment method
1. Understand and practice number representation and conversion in different number systems and perform different arithmetic operations in different number systems.	Quizzes, Exams
2. Recognize, manipulate, simplify, and implement Boolean functions using Boolean algebra theory, K-map and Tabulation Method.	Quizzes, Exams
3. Analyze and design combinational logic circuits using Boolean algebra and logic gates and logic blocks.	Quizzes, Exams
4. Analyze and design computer arithmetic units (full adder, half adder, subtractor, and multiplier).	Quizzes, Exams
5. Analyze and design sequential logic circuits.	Quizzes, Exams
6. Use the Verilog Hardware Description Language (HDL) and use its different modeling techniques for combinational and sequential circuit description.	Assignments
7. Learn how to implement combinational circuits using Programmable devices such as ROM, PAL and PLA.	Assignments, Exams

ABET Outcome
a: Ability to apply mathematics, science and engineering principles. c: Ability to design a system, component, or process to meet desired needs. e: Ability to identify, formulate and solve engineering problems.

Evaluation

Assessment Tool	Expected Due Date	Weight
Midterm Exam	Week9	35 %
Final Exam	End of Semester	45%
HDL Assignments	Week9	10 %
3 Quizzes	3 Quizzes	10 %

Policy	
Attendance	Attendance is very important for the course. In accordance with university policy, students missing more than 10% of total classes are subject to failure. Penalties may be assessed without regard to the student's performance. **Attendance will be recorded** at the beginning or end of each class.
University Policies	Academic honor policy will be enforced, so please read the (honor code). Cheating will not be tolerated, but working together is encouraged
Exams	All exams will be CLOSE-BOOK; necessary algorithms/equations/relations will be supplied as convenient. The date of the Exams will be scheduled later.

ميثاق شرف الأمانة الأكاديمية

بموجب التسجيل في هذا المساق يلتزم الطالب باحترام أنظمة وقوانين الجامعة وخاصة تلك المتعلقة بالأمانة العلمية وعدم الغش .ويتحمل الطالب مسئولية ذاتية، أدبية وقانونية، عن المحافظة على الأمانة العلمية وذلك بالامتناع عن الغش في الامتحانات والوظائف والتقارير، وعدم السماح لغيره من الطلاب بأن ينقلوا عنه في الامتحانات والوظائف والتقارير.

يستوجب الغش أو محاولة الغش التوبيخ والإجراءات القانونية المنصوص عليها في تعليمات الأمانة الأكاديمية التي أقرها مجلس الجامعة بتاريخ 5 تموز 2006 وتشمل ما يلي:

1. **العقوبة الأكاديمية: يقررها مدرس المساق وقد تصل إلى علامة رسوب في المساق.**
2. **العقوبة التأديبية: تقررها لجنة النظام في الكلية وقد تصل إلى الفصل المؤقت أو النهائي من الجامعة.**

بموجب تسجيلي في هذا المساق واستلامي لهذا الميثاق أتعهد أمام الله أن أحافظ على الأمانة الأكاديمية بأن أمتنع عن الغش ،وأن لا أتسامح مع أي محاولة للغش من قبِل الآخرين.