BIRZEIT UNIVERSITY

Electrical and Computer Engineering Department

Summer Semester 2017 Digital Systems (ENCS234) Final Exam

Allowed Time: 150 minutes Date: 29/08/2017 Room: Masri109

Instructor: □ Dr. Abdellatif Abu-Issa □ Dr. Ahmad Alsadeh

Student Name: _____**Student ID**: _____

Question #	Full Mark	Student Mark
Q1	**40**	
Q2	**14**	
Q3	**12**	
Q4	**12**	
Q5	**22**	
TOTAL	**100**	

Note: write your solution on the space provided. If you need more space, write on the back of the sheet containing the question.

Q1] Select the correct answer **(40 points, 2.5 points each):**

1) In octal, the twelve-bit two's complement of the hexadecimal number $2AF_{16}$ is

A. 6522_8

B. 6251_8

C. 5261_8

D. 6521_8

2) Which of the following functions is the constant **1** function?

A. $x' + xy$

B. $xy + x' + xy'$

C. $xy'(x' + y)$

D. $(x' + y)(xy)$

3) Which of the following is equal to $F(x, y) = \sum(m_0, m_0)$

A. $xy + x'y$

B. $x.y' + x'.y$

C. $(x + y')(x' + y)$

D. $(x' + y')(x + y)$

4) How may 2-to-4 decoders with enable input should be used to make a 6-to-64 decoder?

A. 19

B. 18

C. 20

D. 21

5) The following function has ___ Essential prime implicants

A. 2

B. 4

C. 5

D. 8

AB \ CD	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

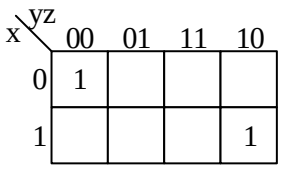
6) Which function is the best for implementing the following function with two level NOR-OR form

A. $F = x'y'z' + xyz'$

B. $F = x'y + xy' + z$

C. $F = (x'y + xy' + z)'$

D. $F = [(x + y + z)(x' + y' + z)]'$



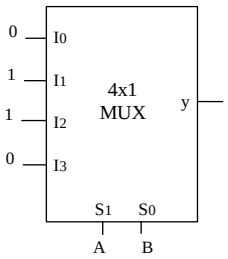
7) The following two circuits have the same functionality of

A. 2-input OR gate

B. 2-input NOR gate

C. 2-input XOR gate

D. 2-input XNOR gate



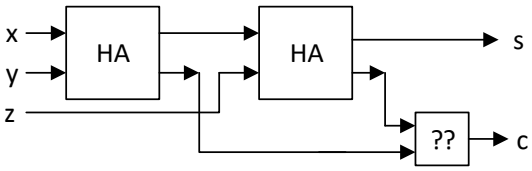
8) Implementation of full adder with two half adders and an ___ gate

A. OR

B. NOR

C. XOR

D. XNOR



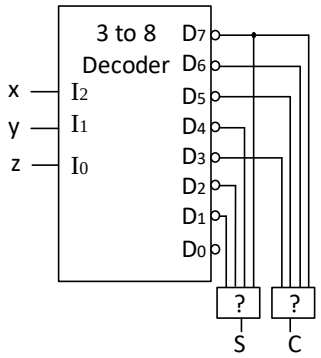
9) Implementation of a full adder with an active low decoder and two

A. OR gates

B. NOR gates

C. AND gates

D. NAND gates



10) Two 'T' Flip-Flops, A and B, are used to implement a sequential circuit. To go from state "$AB = 10$" to "$AB = 11$" we need:

A. $T_A = 0, T_B = 0$

B. $T_A = 0, T_B = 1$

C. $T_A = 1, T_B = 0$

D. $T_A = 1, T_B = 1$

11) If the present state (ABC) is 110, and the input $x = 0$; what will be the next state if the flip flops input functions are:

$\boldsymbol{J_A} = B'x,\ K_A = 1;\quad \boldsymbol{J_B} = A + C'x\ ,\ \boldsymbol{K_B} = xC' + Cx';\quad \boldsymbol{J_C} = Ax + A'B'x'\ ,\ \boldsymbol{K_C} = x$

A. 111

B. 001

C. 010

D. 011

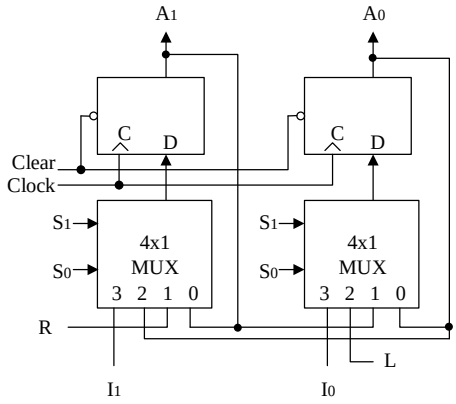
12) If S_1=1, S_0=0 when the Clock is received, then $A_0(t+1)$ and $A_1(t+1)$ will be

A. $A_0(t+1) = L \quad A_1(t+1) = A_0$

B. $A_0(t+1) = A_1 \quad A_1(t+1) = R$

C. $A_0(t+1) = I_0 \quad A_1(t+1) = I_1$

D. $A_0(t+1) = A_0 \quad A_1(t+1) = A_1$



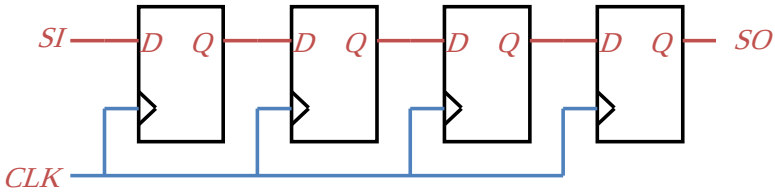
13) Number of data bits that can be stored in the register shown below is _____ and number of clock cycles needed to store data is _____.

A. 4, 1

B. 4, 4

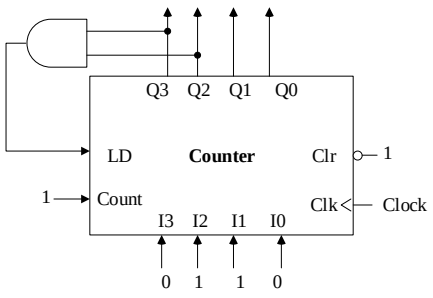
C. 8, 1

D. 8, 4



14) The sequence of counting in decimal for the counter shown below is

Clr	Clk	LD	Count	Operation
x	0	x	x	Clear to 0
1	↑	1	x	Load inputs
1	↑	0	1	Count up
1	↑	0	0	No change



A. 6, 7, 8, 9, 10 , 6 …

B. 12, 11, 10, 9, 8, 7, 6, 12, …

C. 6, 7, 8, 9, 10, 11, 12, 6, …

D. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 0, …

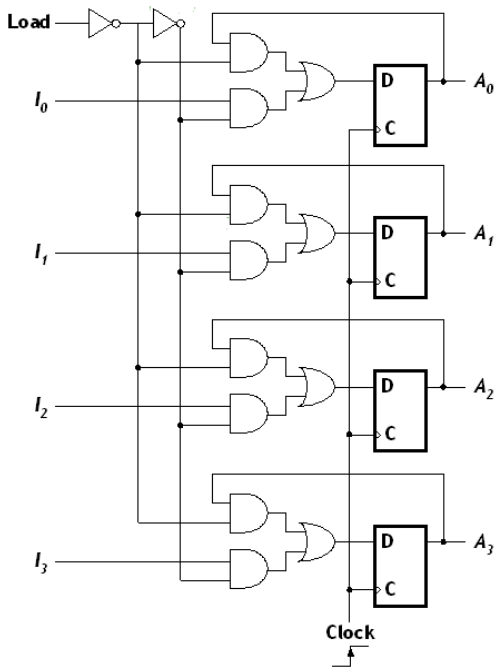
15) If *Load* input is zero, then the circuit will _____ when the clock is received.

A. Count up

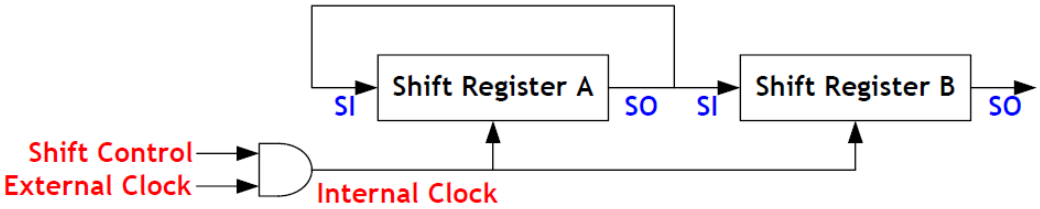
B. count down

C. No change of the state

D. Parallel load the inputs (I_0 ...I_3)



16) The serial transfer shown in Figure below consists of two 4-bit shift registers (*A* and *B*). Assume that the initial contents of registers *A* and *B* is 1011 and 0010 respectively. After 2 clock pulses, what would be the content of registers *A* and *B*.



A. A = 1011 B = 1011

B. A = 1101 B = 1001

C. A = 1110 B = 1100

D. A = 0111 B = 0110

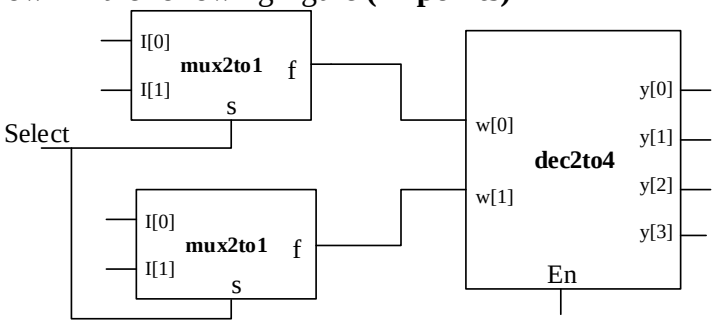
Answering Sheet for Question 1

1)	
2)	
3)	
4)	
5)	
6)	
7)	
8)	
9)	
10)	
11)	
12)	
13)	
14)	
15)	
16)	

Q2] Given the state table below, minimize the number of states using implication chart method. Write down the equivalent states and the reduced table. (**14 points**)

Present State	**Next State**		**Output**	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	F	B	0	0
B	E	G	0	0
C	C	G	0	0
D	A	C	1	1
E	E	D	0	0
F	A	B	0	0
G	F	C	1	1

Q3] For the system shown in the following figure **(12 points)**

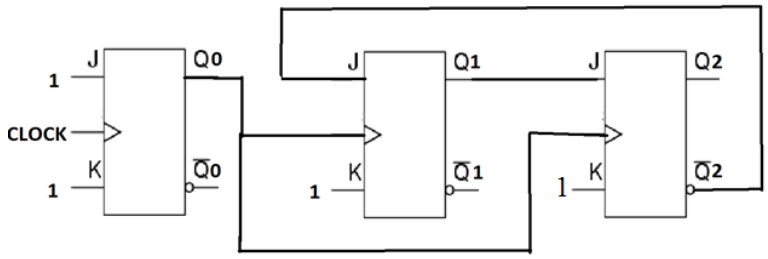


a) (4 pts) Write a Verilog behavioral description for the module `mux2to1`

b) (4 pts) Write a Verilog behavioral description for the module `dec2to4`

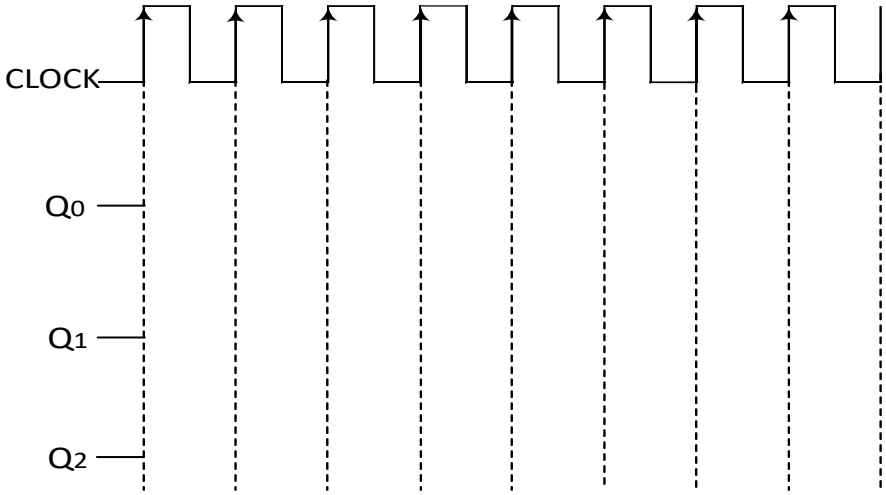
c) (4 pts) Write a Verilog code to describe the whole system structurally from its subsystems

Q4] For the following circuit **(12 points)**



a) (2 pts) Is it ripple or synchronous and why?

b) (6 pts) Draw the timing diagram Starting from ($Q_2Q_1Q_0$=000)



c) (4 pts) Draw the state diagram

Q5] Design a counter circuit that repeats five states in sequence; 000, 010, 011, 101, 110, 000 using D- Flip flops. The circuit is to be designed by treating the unused states as don't-care conditions. **(22 points)**

a) **(2 pts)** Draw the state diagram of the circuit.
b) **(6 pts)** Tabulate the state transition table.
c) **(6 pts)** Derive the state equations for the flip-flops.
d) **(4 pts)** Implement the counter using D- Flip flops and the needed gates
e) **(4 pts)** Analyze the circuit obtained from the design to determine the effect of the unused states. What will happen if a noise signal sends the circuit to one of the unused states?