BIRZEIT UNIVERSITY

Faculty of Engineering & Technology – Electrical & Computer Engineering Department

First Semester 2017-2018 Digital Systems (ENCS234) Final Exam

Allowed Time: 150 minutes Total Marks: 100 Date: 23/01/2018

Student Name :_____

Student ID : _____

ABET Outcome	Question #	Full Mark	Student Mark
	Q#1	20	
	Q#2	17	
	Q#3	20	
	Q#4	20	
	Q#5	23	
	TOTAL	**100**	

Note: write your solution on the space provided. If you need more space, write on the back of the sheet containing the question.

Question#1: 20 Points

Given the following function $F(A,B,C,D) = \sum m(1,2,9,10,13,14,15)$

a) Implement the above function using NOR-NOR implementation. **6 Points**

b) Implement the same function using 4*1 Mux, use A and C on the selection lines. **7 Points**

c) Implement the same function using two decoders 3*8 with external gates as needed. **7 Points**

Question#2: 17 Points

Consider the state table of a sequential circuit is given as below.

Present State	**Next State**		**Output**	
	x = 0	x = 1	x = 0	x = 1
a	b	d	1	0
b	d	g	0	1
c	d	b	1	0
d	e	a	1	0
e	d	c	0	1
f	e	a	1	0
g	d	e	1	0

a) How many Flip Flops are required to implement this circuit without state reductions? Why? **2 Points**

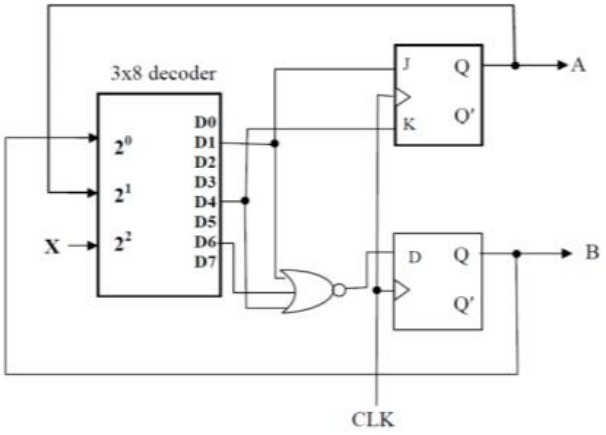
b) Is this circuit a Mealy or Moore Machine? Why? **2 Points**

c) Reduce the state table to a minimum number of states using implication chart method. **10 Points**

d) Draw the reduced state diagram. **3 Points**

Question#3: 20 Points

A. For the sequential circuit shown in figure below derive the state table. **10 Points**



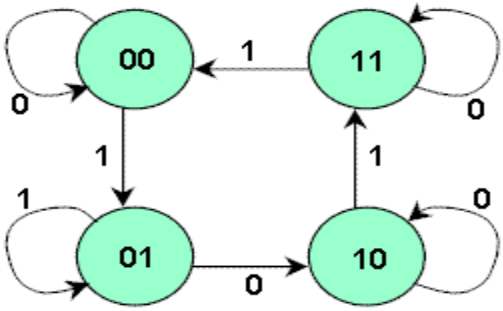
B. Create a state diagram using as a mealy machine for a sequence detector that outputs a 1 when it detects the final bit in the serial data stream 1001. **10 Points**

Example: Inputs: 1 1 1001 1 0 1001001 1 0 …

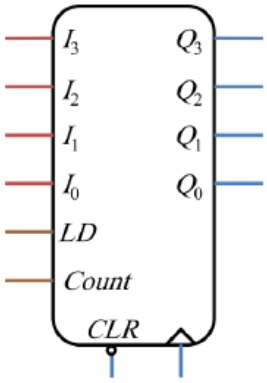
Outputs: 00000 1 00000 1 0 0 1 0 0 …

Question#4: 20 Points

A. Design a synchronous sequential circuit whose state diagram is shown below using TFFs. **10 Points**



B. Using the counter shown below and logic gates design a counter that counts in the sequence 3,4, 5, 6, 7, 8, 9, 10, 11, 12, 3, ... Connect all unused inputs. The counter may cycle through several unwanted states before settling into the final count sequence. Q3 is the most significant bit of the counter output. **10 points**



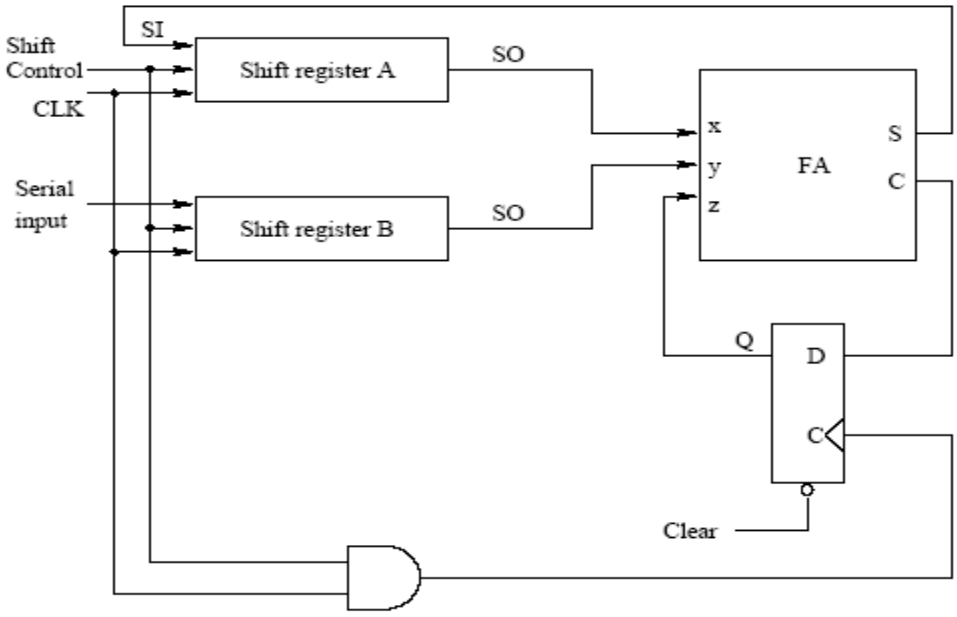
Function Table for the Counter				
CLR	***CLK***	***LD***	***Count***	**Function**
0	x	x	x	Clear to 0
1	↑	1	x	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Question#5: 23 points

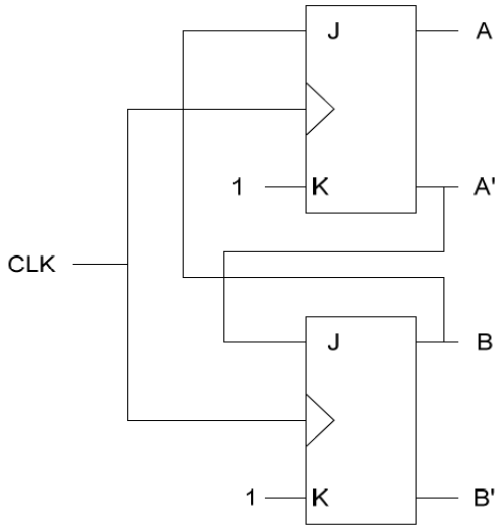
A. The serial adder shown in Figure below consists of two 4-bit shift registers (A and B) and a D flip-flop. Assume that the initial contents of registers A and B is 1001 and 0101, respectively. The sequence of 1011101011 is applied on the serial input of register B, answer the following: **8 Points**

a. After 2 clock pulses, what would be the content of register A and B

b. After 4 clock pulses, what would be the content of register A and B



B. For the following counter circuit shown below



a) What is the count sequence for the above counter? **5 points**

b) 1. Write the HDL code for the JKFF. **5 points**

2. Write a structural HDL for the whole system. **5 points**