If the present state "AB = 01" and the input $x = 0$, what will be the next state if the two T Flip-Flops input functions are

$T_A = B'x$ and $T_B = Ax + A'x'$

Select one:

- a. 10
- b. 01
- c. 00
- d. 11

Time left 1:12:54

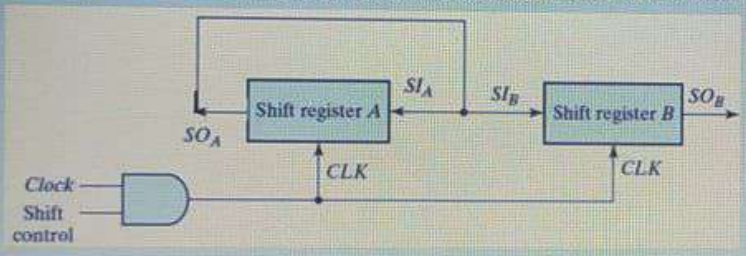
Question 13

Not yet answered

Marked out of 1.00

Flag question

In the circuit below, if both registers A and register B are 16-bit each, then what is the value in hexadecimal of register A after 14 clock pulses. Assume the initial value of A in hexadecimal is 0F0F and the Shift control is active.

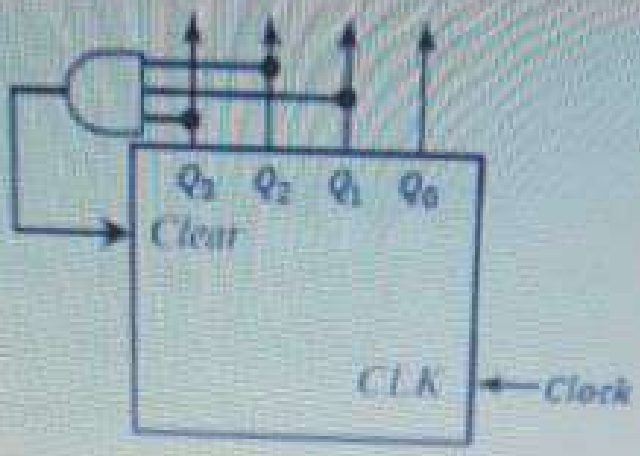


- a. 0F0F
- b. C3C3
- c. 3C3C
- d. 1E1E

Clear my choice

Next page

The complete count sequence of the counter below (in decimal) v
asynchronous clear input is:



a. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, ...

b. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 0, 1, 2, ...

c. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 0, 1, 2, ...

d. 0, 1, 2, 3, 0, 1, 2, ...

e. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 0, 1, 2, ...

0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	1

c.

Present State		Input	Next State		Output
A	B	x	A	B	z
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	1

Clear my choice

Type here to search

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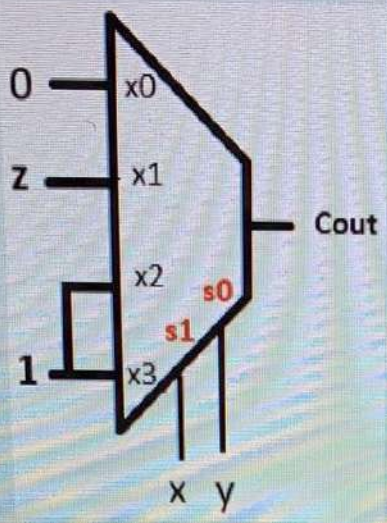
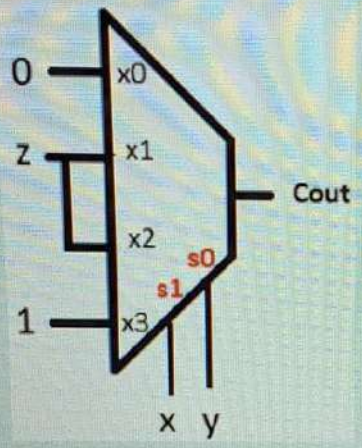
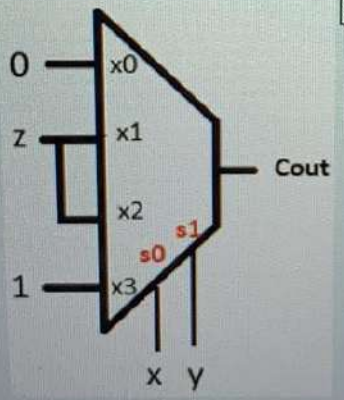


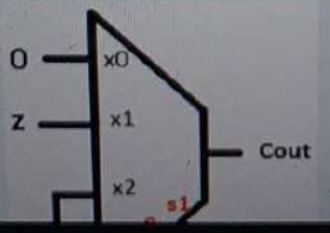
◉ b.



○ c.



○ d.



مشمس غالبًا

Question 7

Not yet answered

Marked out of 1.00

Flag question

.Convert $(1011.101)_2$ to decimal

:Select one

a. $_{10}(11.625)$

b. $_{10}(11.65)$

c. $_{10}(11.25)$

d. $_{10}(9.625)$

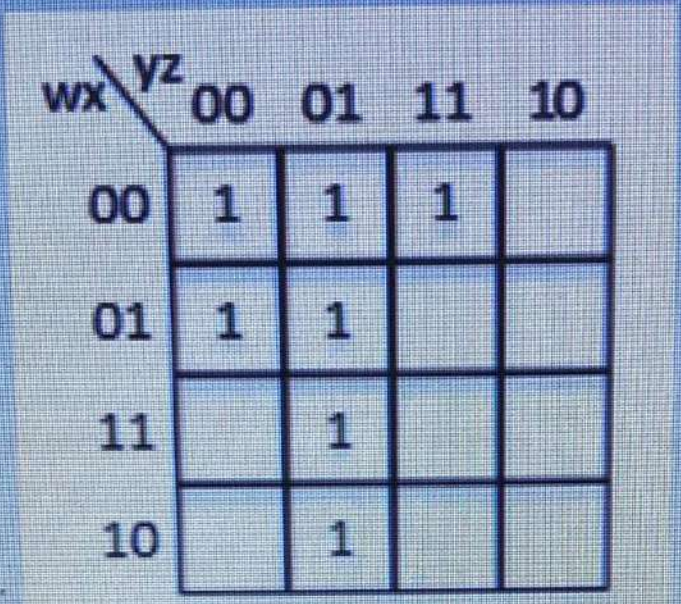
Clear my choice

انتقال إلى...

Second Exam ▶

Time left 1:37:17

For the function F(w,x,y,z), the minimum product of sums (POS) expression



wx \ yz	00	01	11	10
00	1	1	1	
01	1	1		
11		1		
10		1		

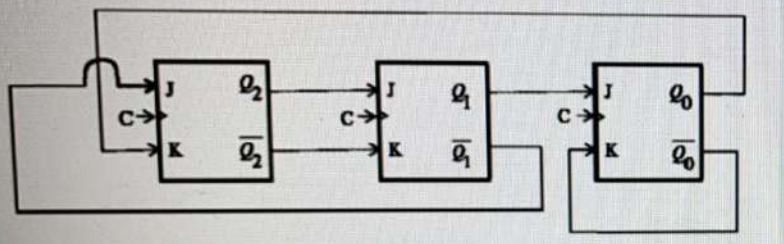
Select one:

- a. $F(w,x,y,z) = (y+z').(w+y).(w+x+z')$
- b. $F(w,x,y,z) = (w'+z).(w'+y').(x'+y').(y'+z)$
- c. $F(w,x,y,z) = (x+y')(w'+x)(w'+z')(w'+y')$
- d. $F(w,x,y,z) = wz'+wy+xy+yz'$

Clear my choice

Time left 1:43:59

The above sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. The state sequence for this circuit for the next 3 clock cycle is:



- a. 001, 010, 011
- b. 100,011,001
- c. 111, 110, 101
- d. 100, 110, 111

Next page

Jump to...

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2)-2-2982000 E-mail : help@ritaj.ps

answered

Marked out of 1.00

Flag question

Present State	Next state		Output	
	X=0	X=1	X=0	X=1
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

Select one:

- a. 4 states
- b. 6 states
- c. 5 states

DELL

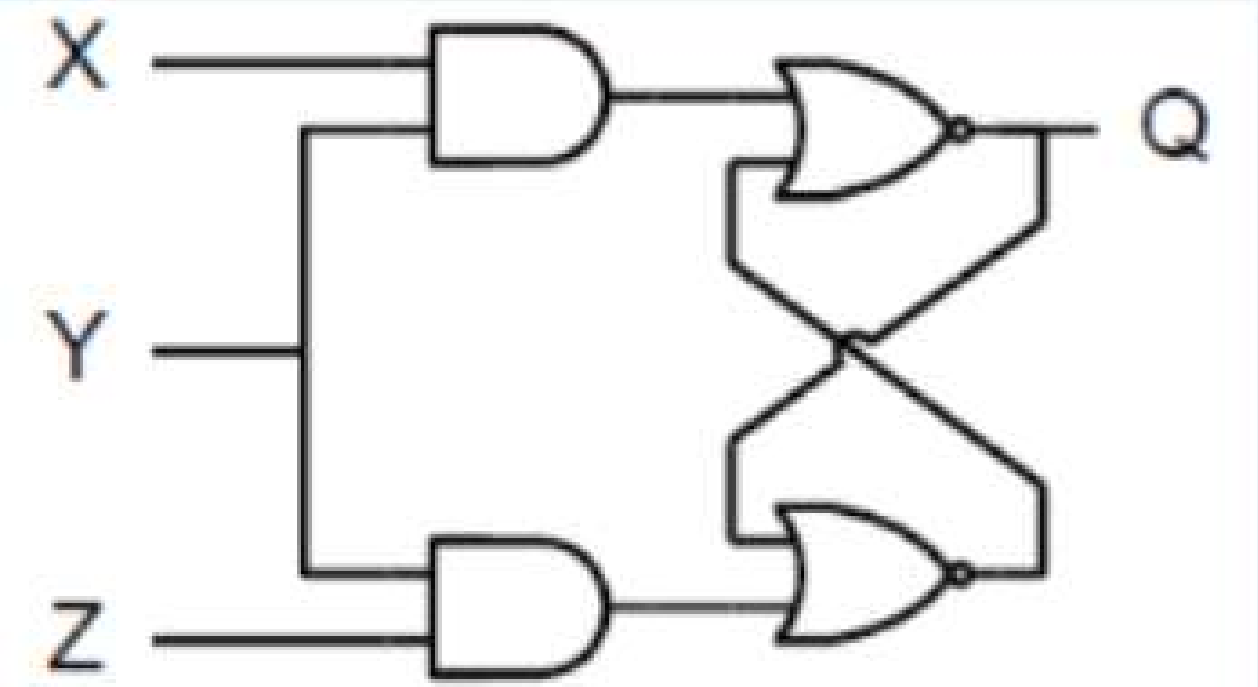
Time left 1:44:03

Communication systems using odd parity for error detection, which of the following sequences received at the destination contains an error.

Msg1= 11000110, Msg2= 11001110, Msg3= 10001110, Msg4= 11001101, Msg5= 11111110, Msg6= 11011110, Msg7= 11001111, Msg8= 11001000

- O a. Msg5, Msg2, Msg7, and Msg8
- O b. Msg1, Msg6, Msg7, and Msg8
- O c. Msg1, Msg2, Msg3, and Msg4
- O d. Msg1, Msg3, Msg4, and Msg6
- O e. Msg1, Msg3, Msg6, and Msg7

To "set" the latch, we should apply



Select one:

- a. X = 0, Y = 1 and Z = 0
- b. X = 1, Y = 0 and Z = 0
- c. X = 1, Y = 1 and Z = 0
- d. X = 0, Y = 1 and Z = 1

TAL SYSTEMS-Lecture-1203 -

Time left 1:4

Give F(A,B,C)= A+B`C, find F` as a standard SOP

- a. A`(C`+B`)
- b. A`B`+A`C`
- c. A`(C`+B)
- d. A`(B`C`)`
- e. A`B+A`C`

Clear my choice

Next pag

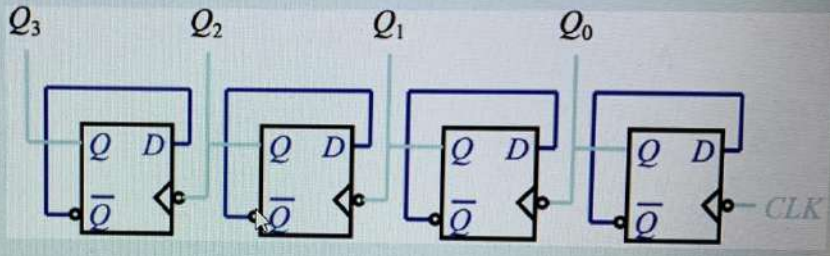
navigation

الوقت المتبقي 1:52:13

3	2	1
11	10	9
19	18	17
27	26	25
35	34	33

Finish attempt

The following sequential circuit represents



:Select one

Count down ripple counter that counts from 0 to 15 .a

Count up synchronous counter that counts from 0 to 15 .b

Count up ripple counter that counts from 0 to 15 .c

Count up ripple counter that counts from 0 to 7 .d

Count down synchronous counter that counts from 0 to 15 .e

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Not
answer
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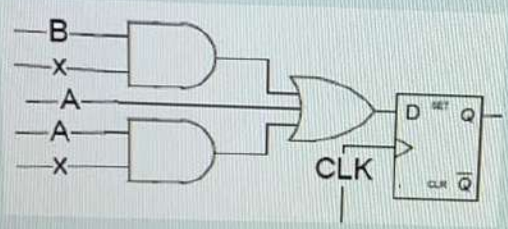
Given the following state table, the circuit implementing A(t+1) is using D Flip-flop

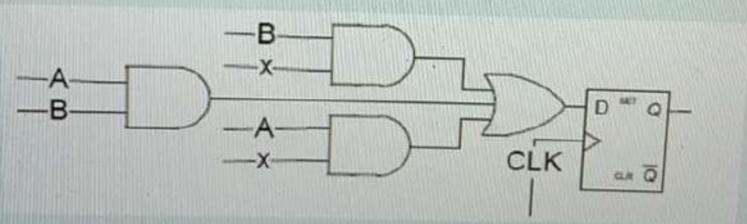
Current State (AB)	Input (x)	Next State (D_AD_B)	Output (z)
00	0	00	0
00	1	01	0
01	0	00	1
01	1	11	0
10	0	00	1
10	1	10	0
11	0	10	1
11	1	11	0

Select one:

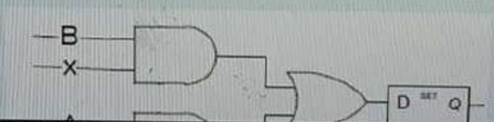
○ a.



◉ b.



○ c.



Question 11

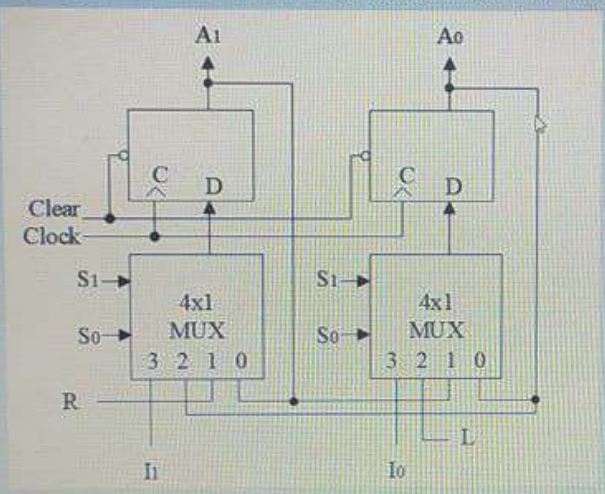
Not yet answered

Marked out of 1.00

Flag question

If S_1=1, S_0=0 when the Clock is received, then A_0 (t+1) and A_1 (t+1) will be

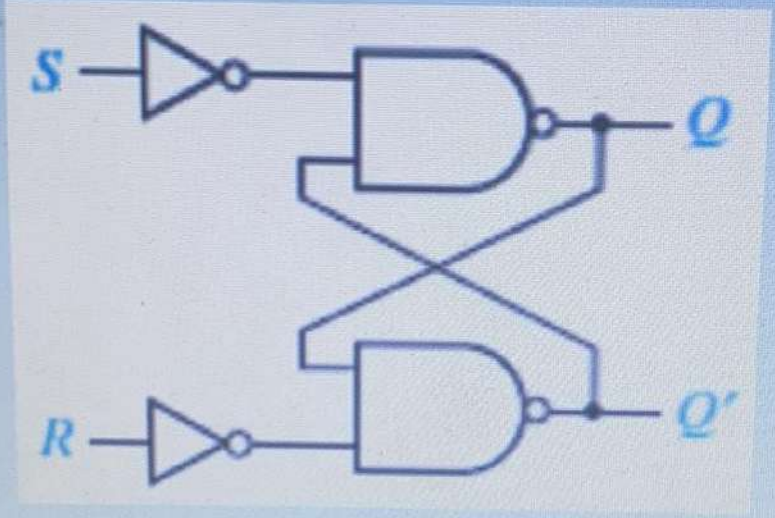
Time left 1:17:59



Select one:

- a. A_0 (t+1)=A_1 . A_1 (t+1)=R
- b. A0 (t+1) =0 A1 (t+1) =1
- c. A_0 (t+1)=I_0 A_1 (t+1)=I_1
- d. A_0 (t+1) =A_0 A_1 (t+1) =A_1
- e. A_0 (t+1)= L A_1(t+1)=A_0

In the following circuit, what happens when S=R=1?



Select one:

- a. No Change
- b. Both outputs Q and Q' are 1
- c. Both outputs Q and Q' are 0
- d. Set
- e. Reset

Clear my choice

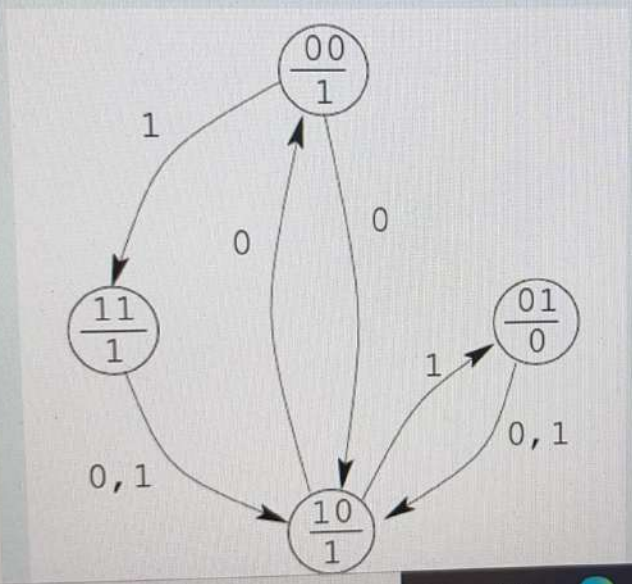
Question 18

Not yet answered

Marked out of 1.00

Flag question

Shown the state diagram for the sequential circuit, which one is the corresponding State Table?



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Time left

Question 12

Not yet answered

Marked out of 1.00

Flag question

Convert this number from one base to another:

$(90E1.01)_{16} = (\quad)_8$

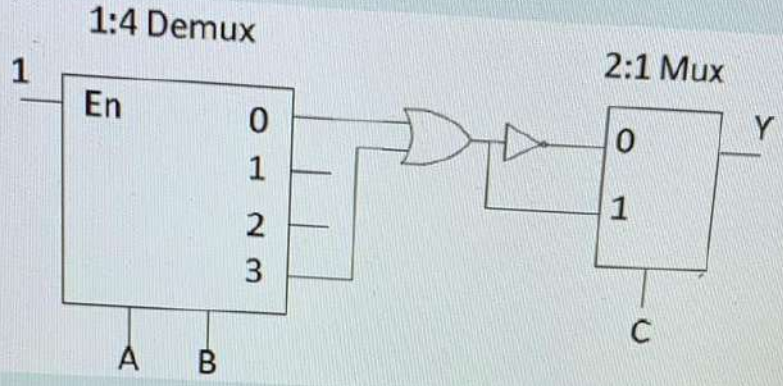
- a. 110341.02
- b. 10341.002
- c. 110341.2
- d. 110341.002
- e. 1103410.02

Next pa

6

t of

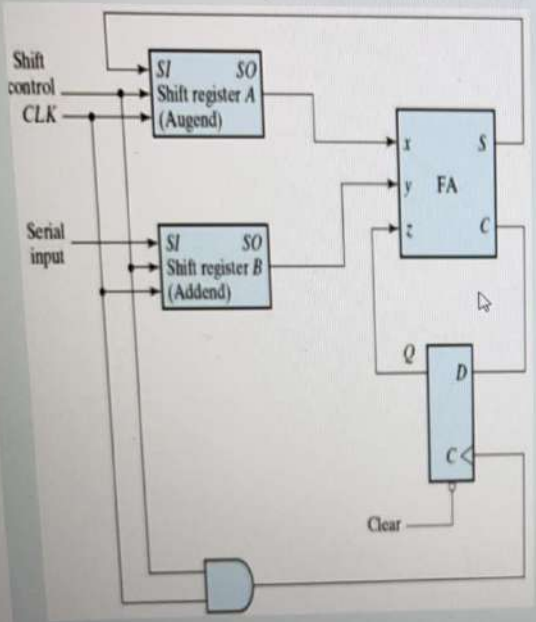
For the circuit below, the Output Y is represents



Select one:

- a. the output carry bit of a full adder
- b. the sum bit of a full adder.
- c. the borrow bit of a full adder
- d. the input carry bit of a full adder

In the circuit below, if both registers A and B are 8-bit each, then what is the value in hexadecimal of registers A after 6 clock pulses. A initial value of A in hexadecimal is 0F and the initial value of B is 5C and the shift control is active.



- a. AC
- b. 3C
- c. 6B
- d. C3

Time

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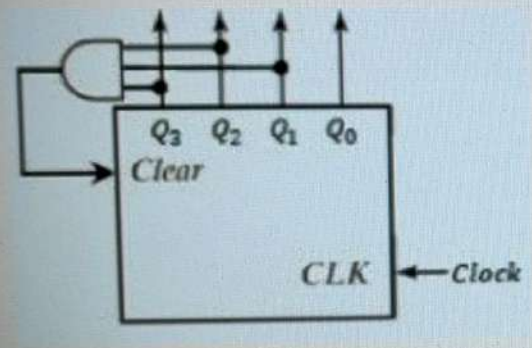
The complete count sequence of the counter below (in decimal) with active -high asynchronous clear input is:



- O a. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 0, 1, 2, ...
- O b. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1,2, ...
- O c. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 0, 1, 2, ...
- O d. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 0, 1, 2, ...
- O e. 0, 1, 2, 3, 0, 1 ,2, ...

Time left 1:27:52

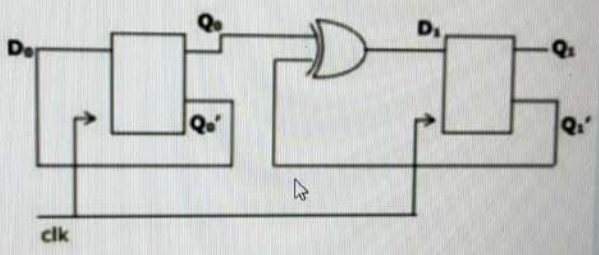
Consider the following circuit the flip-flops are positive edge-triggered D FFs. Each state is designated as a two-bit string Q0Q1. Let the initial state be 00. The state transition sequence is:

A) 00 → 11 → 01

B) 00 → 11

C) 00 → 10 → 01 → 11

D) 00 → 11 → 01 → 10



- a. A
- b. D
- c. B
- d. C

Next page

Time left 1:06:35

Question 21

Not yet answered

Marked out of 1.00

Flag question

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

- a. 00110
- b. 01110
- c. 00001
- d. 00101

Clear my choice

Next page

Time left 0:58:21

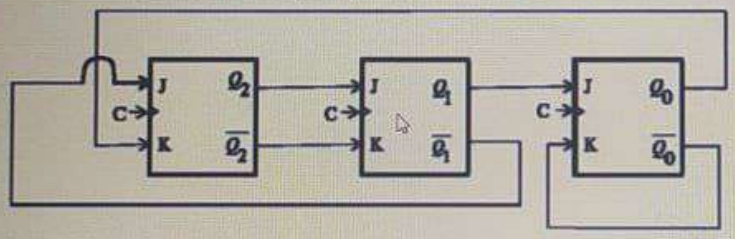
Question 19

Not yet answered

Marked out of 1.00

Flag question

The above sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. The state sequence for this circuit for the next 3 clock cycle is:



- a. 100,011,001
- b. 100, 110, 111
- c. 001, 010, 011
- d. 111, 110, 101

Next page

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Question 17

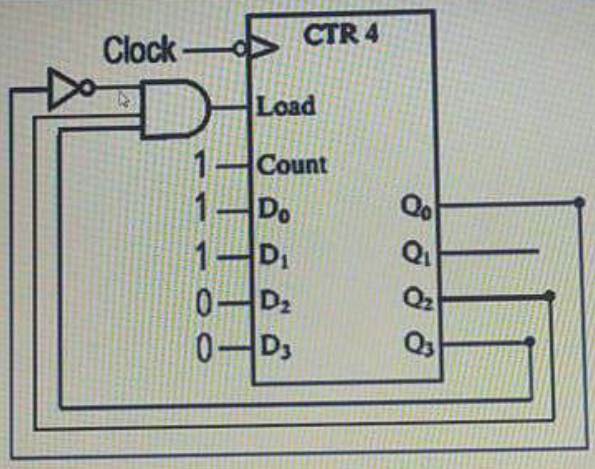
Not yet answered

Marked out of 1.00

Flag question

Time left 1:05:42

The following circuit shows a parallel load binary counter, the range of the counter is



Select one:

- a. 3 to 12
- b. 3 to 7
- c. 3 to 15
- d. 3 to 5

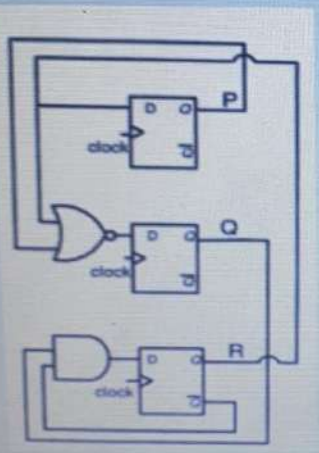
Question 8

Not yet answered

Marked out of 1.00

Flag question

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, **P, Q and R** have a value **0, 1 and 0** respectively, what shall be the value of **P Q R** after the clock edge?



- a. 010
- b. 011
- c. 001
- d. 000

1 2 3
9 10 11
17 18 19
25 26 27
33 34 35

Finish attempt ...

0	1	0	1 0	0
0	1	1	1 0	0
1	0	0	0 0	1
1	0	1	0 1	1
1	1	0	1 0	1
1	1	1	1 0	1

c.

Present State A	B	Input x	Next State A	B	Output z
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	1

Clear my choice

الوقت المتبقي 1:47:31

The result **in BCD** of the following?

$(599)_{10} + (984)_{10}$

.a 1010110000011

.b 0001010110000011

.c 111010011101

.d 1000010110000011

.e 001010110000011

Clear my choice

Next page

Question 7

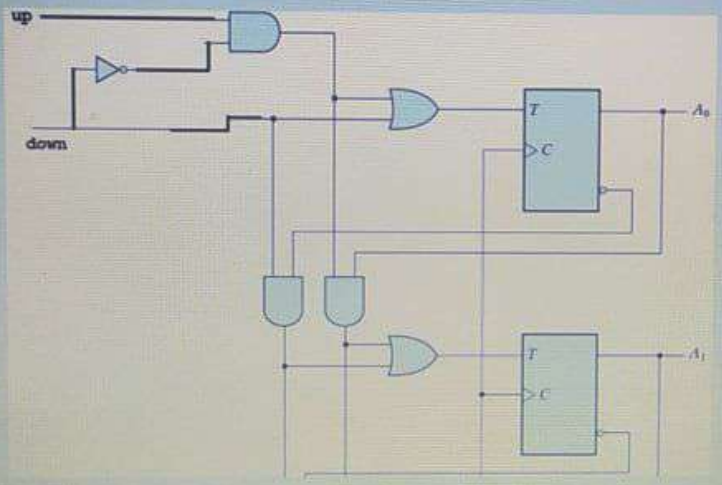
Not yet answered

Marked out of 1.00

Flag question

In the UP/DOWN counter below, which control signal has the priority up or down?

Time left



- a. depends on the mode of operation
- b. down
- c. up
- d. same priority

Given the table below for a given sequential circuit to be designed using JK flip-flops, the equation of the J input of flip-flop A is:

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0			0			
0	0	1			X			
0	1	0			X			
0	1	1			X			
1	0	0			X			
1	0	1			X			
1	1	0			X			
1	1	1			X			

- a. $J_A = X+A+B$
- b. $J_A = X`A`B`$
- c. $J_A = 1$
- d. $J_A = 0$

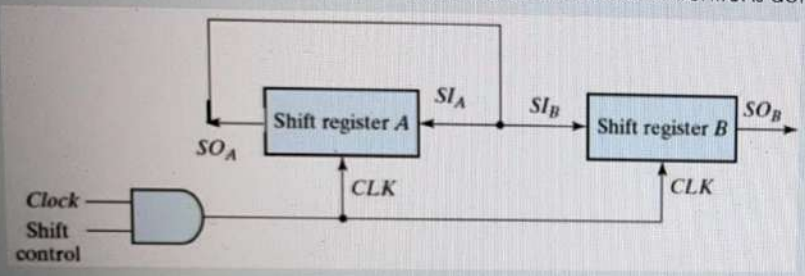
The result **in BCD** of the following?

$(599)_{10} + (984)_{10}$

- a. 1000010110000011
- b. 111010011101
- c. 000101011000011
- d. 101011000011
- e. 001010110000011

Time left 1:48:29

In the circuit below, if both registers A and register B are 16-bit each, then what is the value in hexadecimal of register A after 14 clock pulses. Assume the initial value of A in hexadecimal is 0F0F and the Shift control is active.



- O a. 1E1E
- O b. 0F0F
- O c. C3C3
- O d. 3C3C

Next page

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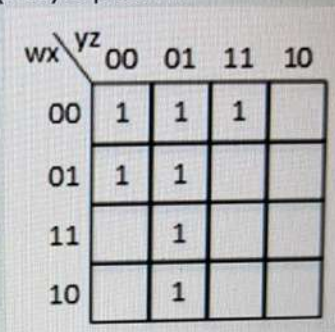
Flag
question

For the function F(w,x,y,z), the minimum product of sums (POS) expression



wx \ yz	00	01	11	10
00	1	1	1	
01	1	1		
11		1		
10		1		

Select one:

- a. $F(w,x,y,z) = wz'+wy+xy+yz'$
- b. $F(w,x,y,z) = (y+z').(w+y).(w+x+z')$
- c. $F(w,x,y,z) = (x+y')(w'+x)(w'+z')(w'+y')$
- d. $F(w,x,y,z) = (w'+z).(w'+y').(x'+y').(y'+z)$

Clear my choice

Time left

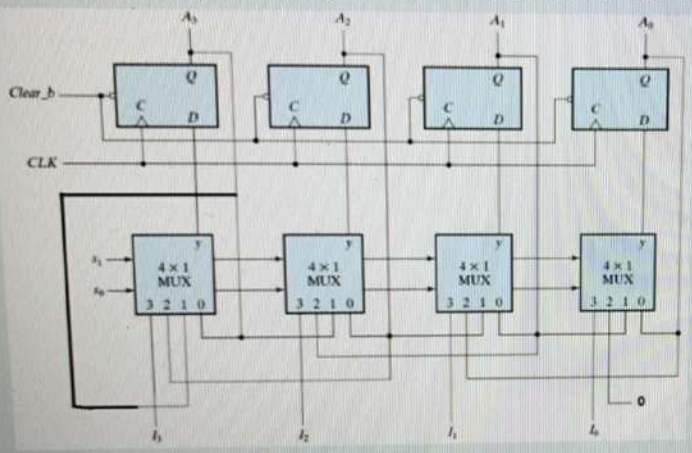
Question 14

Not yet answered

Marked out of 1.00

Flag question

What will be the output of the register below after 2 clock pulses, if its initial values are 1100 in binary and S1S0=01



- a. 0101
- b. 0011
- c. 0000
- d. 1111

Clear my choice

Given the table below for a given sequential circuit to be designed using JK flip-flops, the equation of the J input of flip-flop A is:

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0			0			
0	0	1			X			
0	1	0			X			
0	1	1			X			
1	0	0			X			
1	0	1			X			
1	1	0			X			
1	1	1			X			

- a. $J_A = 1$
- b. $J_A = X+A+B$
- c. $J_A = 0$
- d. $J_A = X`A`B`$

Clear my choice

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If the present state "AB = 01" and the input $x = 0$, what will be the next state if the two T Flip-Flops input functions are $T_A = B'x$ and $T_B = Ax + A'x'$

Select one:

- a. 00
- b. 10
- c. 01
- d. 11

Clear my choice

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A demultiplexer is used to ...

- [ ] a. Select data from several inputs and route it to single output
- [x] b. Perform serial to parallel conversion
- [x] c. Route the data from single input to one of many outputs
- [ ] d. None is correct
- [ ] e. All is correct

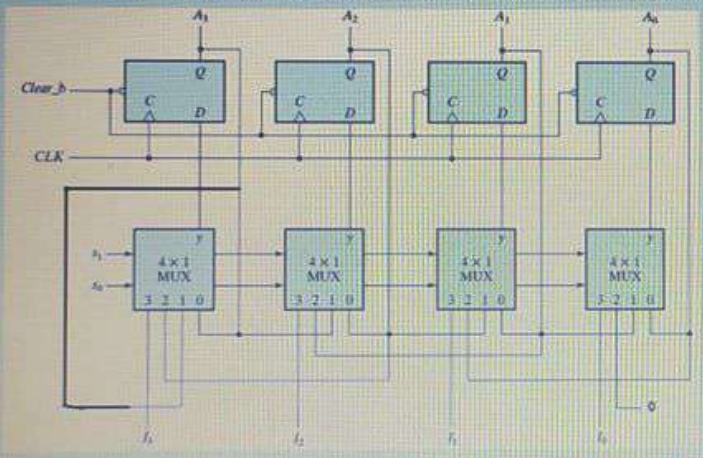
Question 2

Not yet answered

Marked out of 1.00

Flag question

What will be the output of the register below after 2 clock pulses, if its initial values are 1100 in binary and S1S0=01



a. 0101

b. 1111

c. 0000

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الوقت المتبقي 1:52:37

The complement of the function: **F= x+1 + (y`x` + z)`**

y`x`+z .a

1 .b

x`+0 + (y`x` + z) .c

0 .d

Clear my choice

Question 1
Not yet answered
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Flag question

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انتقال إلى...

Second Exam ▶

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

- a. 00110
- b. 01110
- c. 00001
- d. 00101

Clear my choice

Convert this number from one base to another:

$(.711)_8 = (\quad)_2$

- a. .111001001
- b. .1110010011
- c. .1110101
- d. .011001001
- e. .01111001001

Clear my choice

The canonical form for F(A, B,C) based on the truth table below is

A	B	C	F
0	0	0	**1**
0	0	1	**X**
0	1	0	**1**
0	1	1	**0**
1	0	0	**0**
1	0	1	**X**
1	1	0	**0**
1	1	1	**X**

Select one:

- a. ΠM(3,4,6)*d(1,5,7)
- b. ΠM(0,1,2)*d(1,5)
- c. Σm(3,4,5,6)+d(1,7)
- d. Σm(0,2,5)+d(1,5)

Clear my choice

Question 1

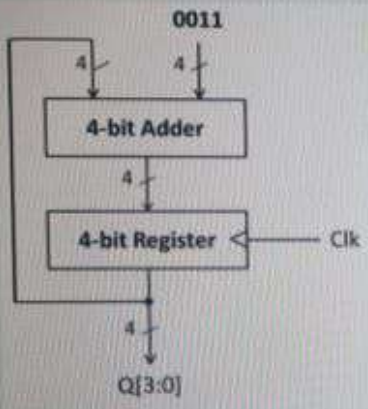
Not yet answered

Marked out of 1.00

Flag question

Time left 1:51:18

Given the following block diagram: If the output Q[3:0] is 0011 during the current cycle I, shown the output Q at (I+2) after 2 cycles.



Select one:

- a. 0011
- b. 1011
- c. 0111
- d. 1101
- e. 1001

Write characteristic equation to construct T-FF from a JK-FF is:

- a. $Q^+ = T \odot Q$
- b. $Q^+ = T`Q` \oplus TQ$
- c. $Q^+ = TQ` + T`Q$
- d. $Q^+ = T`Q` . TQ$
- e. $Q^+ = TQ` \oplus T`Q$