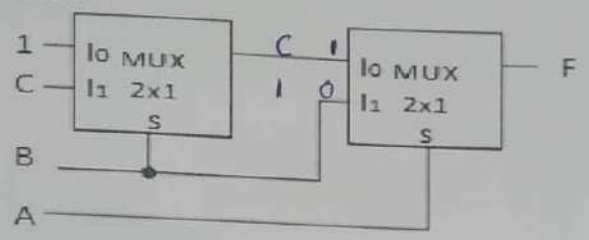
5. The circuit represents the Boolean function

A. F(A,B,C) = ABC + A`B`
B. F(A,B,C) = AB + A`C
C. F(A,B,C) = A`C + A`B`
D. F(A,B,C) = AB + A`C + A`B`
E. None



16. Convert this number from one base to another:

$(90E1.01)_{16} = (\quad)_8$

A. 110341.02
B. 110341.2
C. 1103410.02
D. 110341.002
E. 10341.002

17. Find the complement of the function in minterm list form:

$F(a,b,c) = \Pi(0,1,2,4,6)$

A. $\Sigma(0,1,2,4,6)$
B. $\Pi(3,5,7)$
C. a`bc +a`bc`+abc
D. (a`+b+c)(a`+b+c`)(a+b+c)
E. $\Sigma(3,5,7)$

18. Consider the following boolean functions:

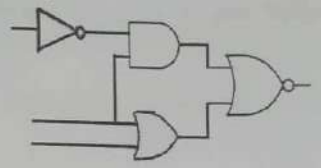
F(A,B,C)= A` + B`

G(A,B,C) = Σ (2,3,5,7)

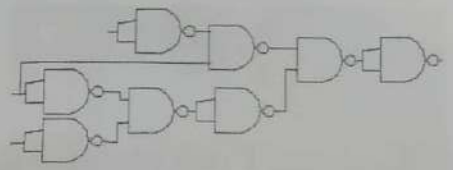
Express this function: (F + G`) in a product of maxterm form:

A. A+B+C
B. A`+B`+C`
C. A`B`C`
D. ABC
E. A`+B`+C

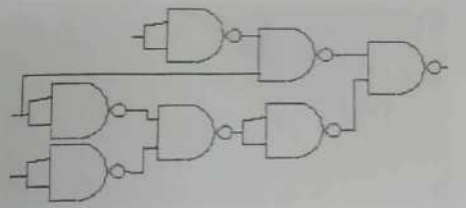
19. Redesign the following circuit using **NAND** gate(s) only:



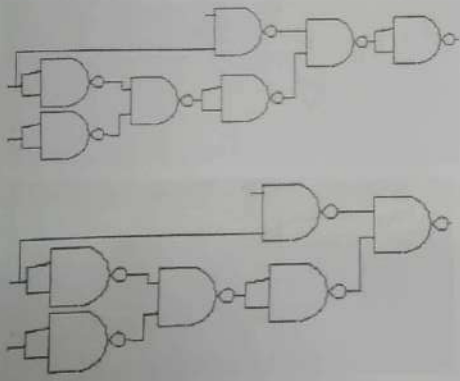
A.



B.



C.



D.

E) None

20. After minimizing F(A,B,C,D), given in the k-map as a sum of products, what's the value of F(0,0,1,0)?

A. AB`
B. 1
C) 0
D. X
E. None

AB \ CD	00	01	11	10
00	0	1	1	X
01	1	1	0	0
11	1	1	0	0
10	1	1	X	0

$B\bar{C} + \bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$

Question#2: (14 points)

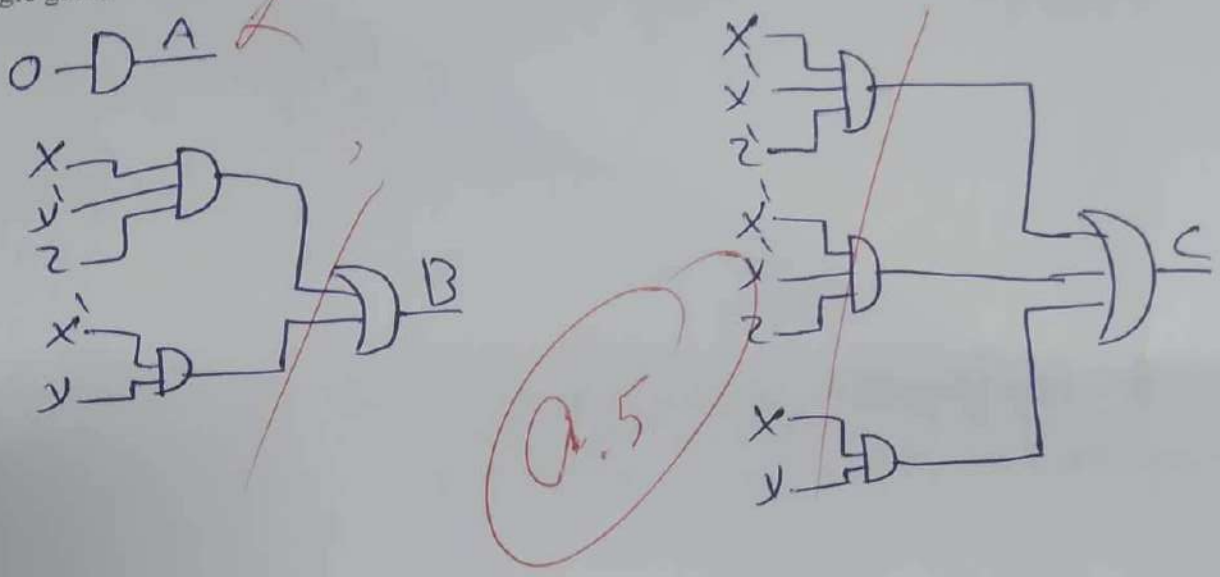
Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

1) (4 **points**) Derive the truth table that defines the required relationship between inputs and outputs.

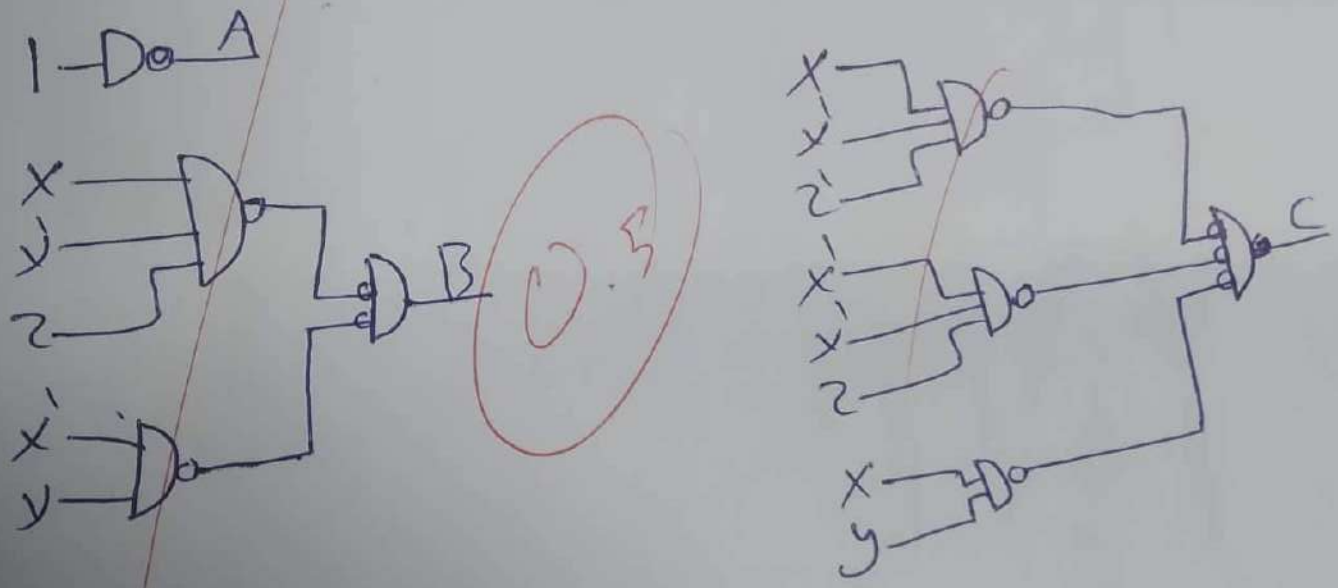
x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	0	0

2) (4 **points**) Obtain the simplified Boolean functions for each output as a function of the input variables.

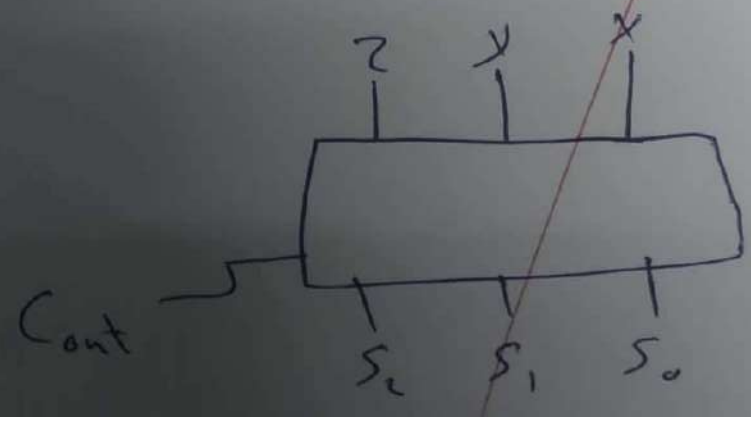
3) (2 **points**) Draw the logic diagram for the Boolean functions in (2) using NOT, AND and OR logic gates.



4) (2 **point**) Draw the logic diagram for the Boolean functions in (2) using NAND logic gates only.



5) (**2 points**) Implement the 3 Boolean functions using a full adder circuit.



Question#3: (14 points)

Using 2×4 decoders and one 4×1 multiplexer, design a circuit with the following properties: It has two inputs with 2-bit each (x_1 x_0) (y_1 y_0) and has 2 inputs, f_1 f_0 to select the function of the circuit:

- *EQ* outputs 1 if the two inputs are equal
- *GT* outputs 1 if X is larger than Y
- *LTE* outputs 1 if X is smaller or equal to Y
- *NULL* outputs 0

You need to show (1) the truth table for the decoders, (2) the truth table for the multiplexer, and (3) the final circuit implementation of the whole design. You must use a minimum number of 2×4 decoders with enables (i.e., if enable is 0 all outputs are 0, otherwise, the output is 1 for the minterms), only one 4×1 multiplexer, and the minimum number of additional gates (wide gates are allowed to be used in the implementation).

Show the circuit diagram with all the **pins to the decoders and multiplexer labeled properly**. State any assumption you are making in your design.

Decoder 2×4

A_0 A_1 A_2 A_3

Mux 4x1 F

A B C D

0 0 0 0

4

Question#4: (12 points)

(**10 points**) An 8×1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1, and S_0, respectively. The data inputs I_0 through I_7, are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Determine the Boolean function that the multiplexer implements.

9

$F = D$, $S_2 = 000$

$F = 0$, $S = 001$

$F = 0$, $S = 010$

$F = 1$, $S = 011$

$F = D$, $S = 100$

$F = 1$, $S = 101$

Question 1: (**60 points**, 3 points each). Select the correct answer

1	2	3	4	5	6	7	8	9	10
D	A	D	A	A	C	B	E	A	E

11	12	13	14	15	16	17	18	19	20
A	F	E	B	E	D	E	B	E	C

1. The below number is in 2's complement, what's the value of this number in decimal?

$(1011)_2$

0100
+1
0101

A. 13
B. 19
C. -19
D. -5
E. 11
F. -11

2. Find the canonical sum-of-products (SOP) of the standard function:

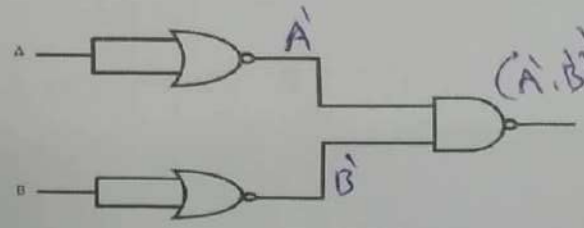
F(x,y,z) = xy`+yz`

$xy'z + xy'\grave{z} + xy\grave{z} + \grave{x}yz'$
101 100 110 010
5 4 6 2

A. Σ(2,4,5,6)
B. Π(2,4,5,6)
C. Σ(0,1,3,7)
D. Π(0,1,3,6,7)
E. None

3. Which logic function does this circuit generate?

A. AND
B. NAND
C. NOR
D. OR
E. XOR



A	B	
0	0	0
0	1	1
1	0	1
1	1	1

4. Express the function F as a sum-of-products (SOP):

$F = A (B \oplus C)' + D$

$A(B'C + BC')' + D$

$A((B+C').(B'+C)) + D$

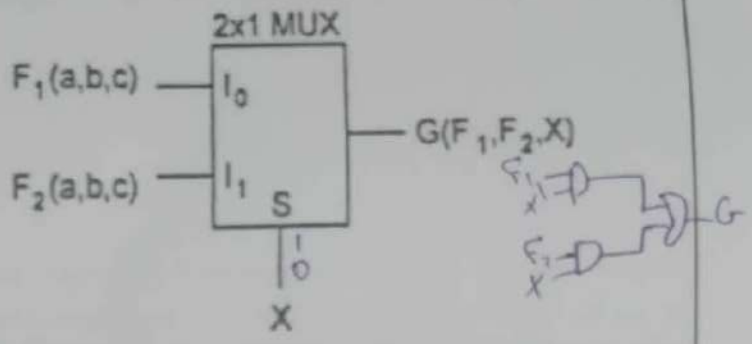
$A\cancel{BB} + ABC + AC'B' + A\cancel{AC} + D$

$ABC + AB'C' + D$

A. $F = ABC + AB'C' + D$
B. $AB'C + ABC' + D$
C. $F = ABCD + AB'C'D$
D. $F = A (B'C + BC' + D)$
E. $F = AB'C + ABC' + AD$

5. Consider the following diagram. Represent the function G in terms of F1(a,b,c), F2(a,b,c) and X.

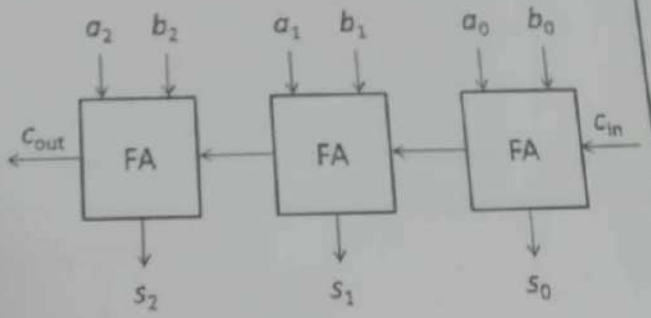
A. $X' F1 + X F2$
B. $X' F1 + X F2'$
C. $X F1 + X' F2$
D. $X' F1' + X F2$
E. $X' F1 + F2$



6. Consider the following diagram of a 3-bit adder:

What is the value of s_2, s_1, s_0 and C_{out}, if $a_2\ a_1\ a_0 = 101$ and $b_2\ b_1\ b_0 = 110$ and $C_{in} = 0$?

A. $s_2\ s_1\ s_0 = 011$ and $C_{out} = 0$
B. $s_2\ s_1\ s_0 = 010$ and $C_{out} = 1$
C. $s_2\ s_1\ s_0 = 011$ and $C_{out} = 1$
D. $s_2\ s_1\ s_0 = 001$ and $C_{out} = 1$
E. $s_2\ s_1\ s_0 = 0110$ and $C_{out} = 1$



1 1 0
1 0 1 +
1 0 1 1
Carry

7. Assume that $F(A,B,C) = \Pi(1,2,3,6)$ and $G(A,B,C) = \Sigma(0, 2, 4, 6)$, The expression of the function $F'G$ as a sum-of-minterms is

$F = m_0 + m_4 + m_5 + m_7$

$(m_0 + m_4 + m_5 + m_7) \cdot (m_0 + m_2 + m_4 + m_6)$

A. m1+m6
B. m2+m6
C. m2+m4
D. m1+m2
E. m2+m7

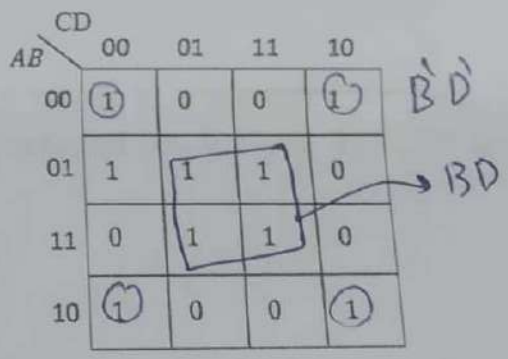
Convert this number from one base to another:

$(20)_{16}$ = ( )$_{BCD}$

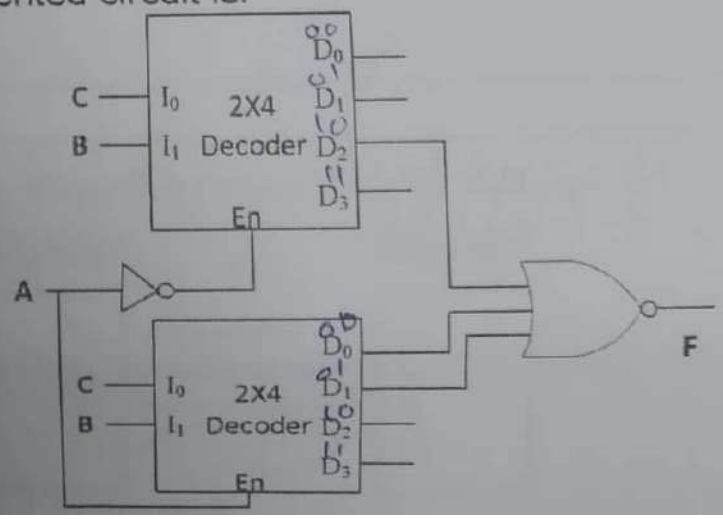
A. 001100100
B. 00110010
C. 00010010
D. 001100110
E. 00100000

9. The size of the smallest multiplexer that can be used to implement any function of the form F(A,B,C,D) without any other logic gates (not even inverters) is:
   A. 2x1
   B. 4x1
   C. 16x1
   D. 32x1
   E. 8x1

10. Consider the following boolean functions, list all essential prime implicants in the following k-map:
   A. BD
   B. B`D`
   C. BD, B`D`, A`C`D`
   D. A`C`D`
   E. BD, B`D`



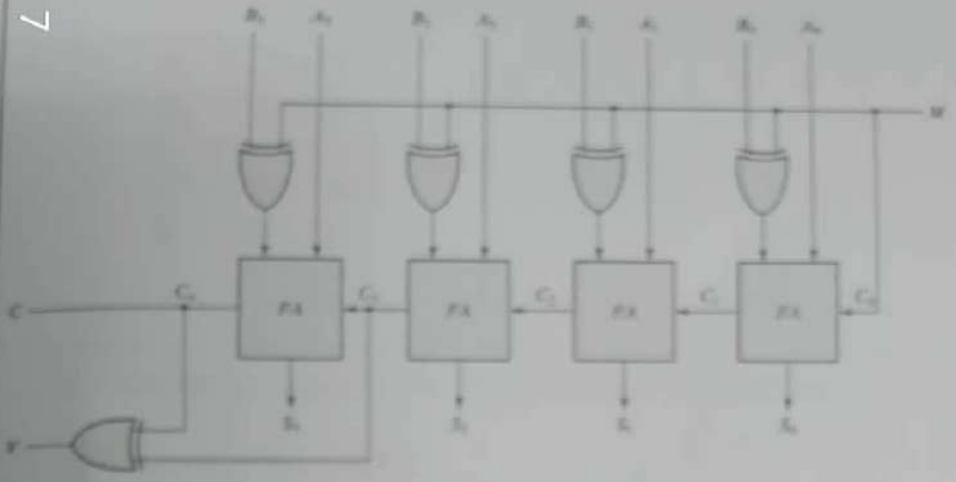
11. The function F(A,B,C) of this implemented circuit is:
   A. F = ∑(0, 1, 3, 6, 7)
   B. F = ∑(1, 3, 6, 7)
   C. F = ∑(0, 1, 3, 6)
   D. F = ∑(0, 1, 6, 7)
   E. None



A B C | F
0 0 0

12. A demultiplexer is used to ...
   A. Route the data from single input to one of many outputs
   B. Select data from several inputs and route it to several outputs
   C. Select data from several inputs and route it to single output
   D. A and B are correct
   E. All are correct
   F. None are correct

13. Consider the following diagram of a 4-bit adder/ subtractor:



Configure the value of M, A_3, A_2, A_1, A_0 the above circuit to implement 4-bit 2's complement, such that the input is B_3 B_2 B_1 B_0, and the output S_3 S_2 S_1 S_0= (2's of (B_3 B_2 B_1 B_0))

   A. A3=1, A2=1, A1=1, A0=1, M=1
   B. A3=0, A2=0, A1=0, A0=0, M=1
   C. A3=0, A2=0, A1=0, A0=0, M=0
   D. A3=1, A2=1, A1=1, A0=1, M=0
   E. A3=1, A2=0, A1=0, A0=0, M=1

14. Assume that I_0 has the lowest priority, show the output Y_1Y_0 for $X_2X_1X_0$= 111
   A. 01
   B. 11
   C. 10
   D. 00
   E. None