Abdallah Fialak

1	2	3	4	5	6	7	8	9	10	11	12	13	14
b	b	c	c	c	b	e	a	a	c	c	c	e	BB

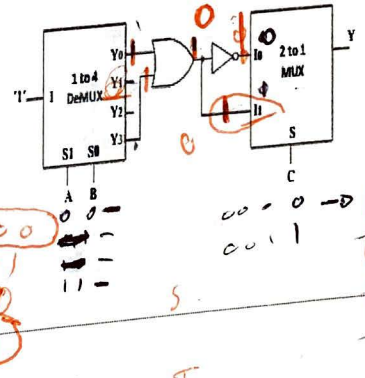
Question#1] Select the correct answer (**42 points, 3 points each**):

1. Convert the following BCD number to decimal $(100000000011)_{BCD}$
   a. 8003
   b. 803
   c. 1003
   d. 103
   e. None

2. Converting $(0111011.100)_2$ to base 16 yields which of the following results?
   a. 3C.4
   b. 3B.8
   c. 73.4
   d. 3B.4
   e. None

3. The simplification of the Boolean function $(\overline{ABC}) + (\overline{ABC})$
   a. A
   b. BC
   c. 1
   d. 0
   e. None

4. The output Y of the circuit computes
   a. $Y(A,B,C) = \sum(1,2,3,4,7)$
   b. $Y(A,B,C) = \sum(3,5,6,7)$
   c. $Y(A,B,C) = \sum(1,2,4,7)$
   d. $Y(A,B,C) = \prod(2,3,6)$
   e. None



5. For the shown circuit the function F is

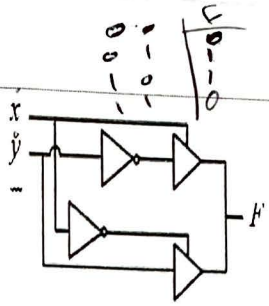
a. F = X AND Y

b. F = X OR Y

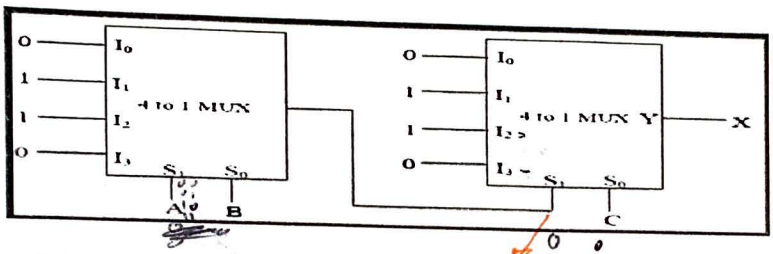
c. F = X XOR Y

d. F = X XNOR Y

e. None



6. In the following circuit, **X** given by



a. X (A,B,C) = ∑ (0,3,5,6)

b. X (A,B,C) = ∑ (1,2,4,7)

c. X (A,B,C) = ∏(1,2,4,7)

d. X (A,B,C) = ∏ (0,6)

e. None

7. Identify the function which generates the K-map shown

a. F(A,B,C) = ∑(1,3,4,7)

b. F(A,B,C) = ∏(1,3,4,7)

c. F(A,B,C) = ∑(1,3,5,6)

d. F(A,B,C) = ∏(1,3,5,6)

e. None

C \ AB	00	01	11	10
0	0	0	1	0
1	1	1	0	1

8. The circuit has the same functionality for input A, B

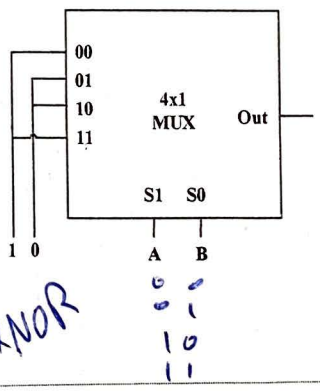
a. XNOR

b. XOR

c. NAND

d. NOR

e. None



9. In the shown circuit, the implementation of

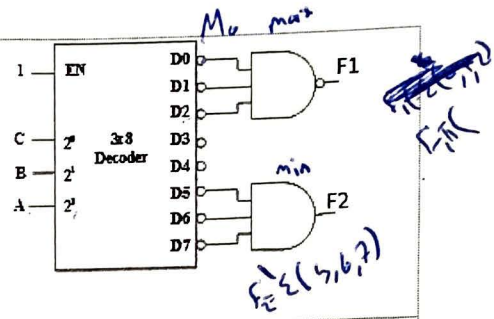
a. F1 = ∑(0,1,2) , F2 = ∑(5,6,7)

b. F1 = ∑(0,1,2), F2 = ∑(5,6,7)

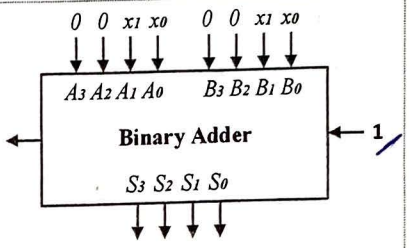
c. F1 = ∏(1,2,3), F2 = ∏(5,6,7)

d. F1 = ∑(1,2,3), F2 = ∑(5,6,7)

e. None



10. In the shown circuit, given "X" is a 2-bit binary number (x_1x_0):



a. *Sum = X*

b. *Sum = 2 X*

c. *Sum = 2 X + 1*

d. *Sum = 2 X + 2*

e. *None*

11. Converting $(310)_4$ to decimal answer is:

$3\times4^2 + 1\times4^1 + 0\times4^0$

$48 + 4 + 0 = 52$

a. 130

b. 132

c. 52

d. 140

e. None

12. The base of the numbers in the operation $(24 + 17 = 40)$ to be correct is

17
24
40

a. 9

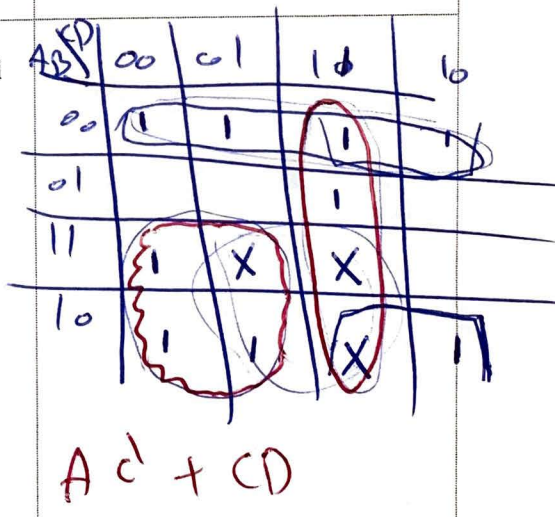
b. 10

c. 11

d. 12

e. None

13. Consider the $F(A,B,C,D) = \sum(0,1,2,3,7,8,9,10,12)$ with don't care terms $d(A,B,C,D) = \sum(11,13,15)$. List all of the essential prime implicants



a. B', AD, AC', CD

b. B', AC', CD

c. AD, AC', CD

d. B', AD, CD

e. None

14. Implementation of full adder with two half adders and an ___ gate

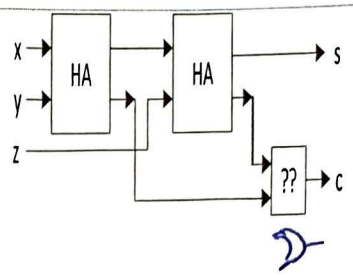
A. NOR

B. OR

C. XOR

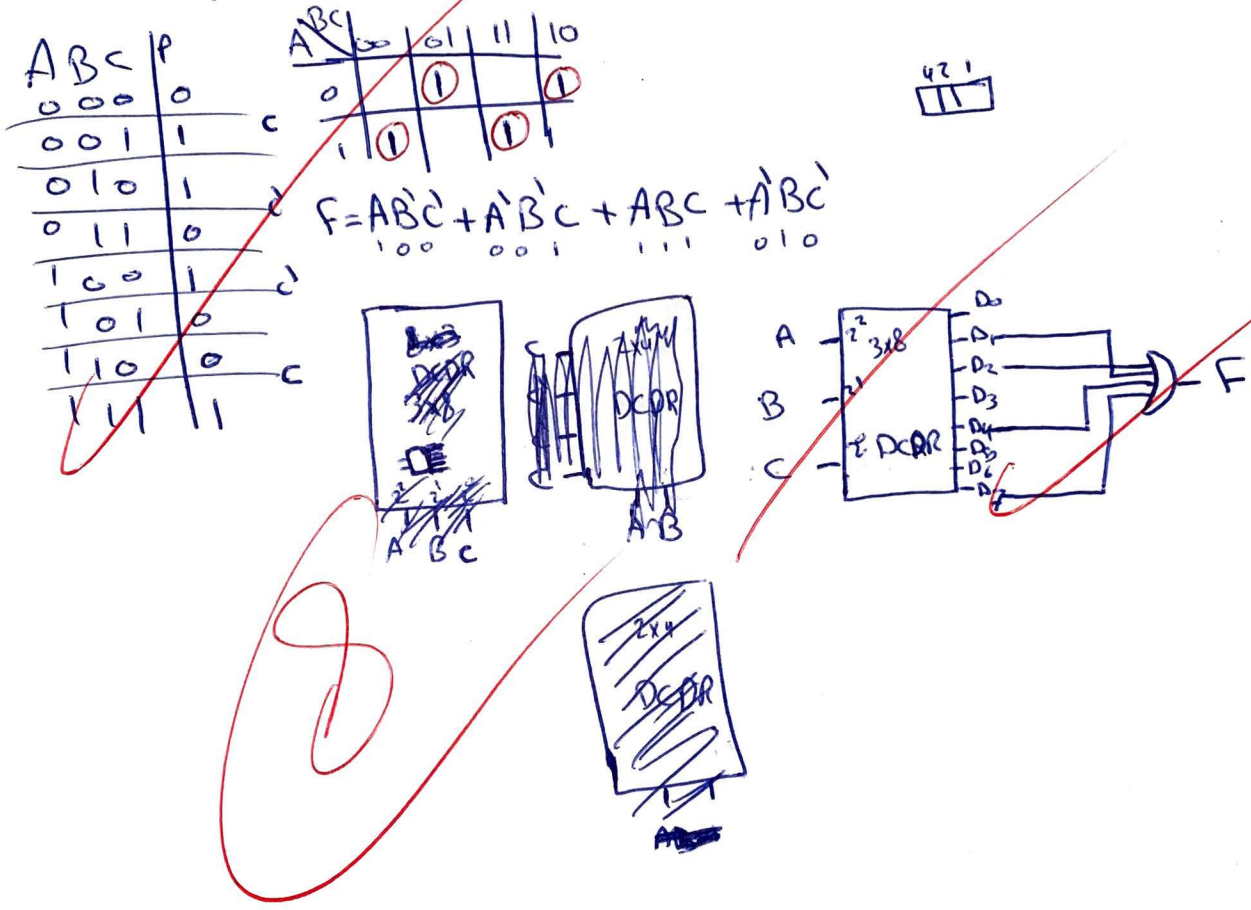
D. XNOR

E. None



Question#2] 15 points

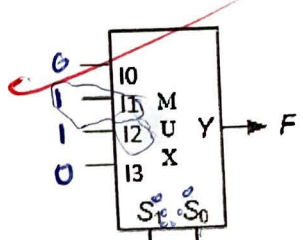
A. Use a suitable size decoder and an external logic gate to implement the even parity generator for a circuit with three inputs A, B, C **(8 points)**



B. The following circuit is used to implement the Boolean function $F(A,B,C) = \Sigma(3, 6)$ Determine the inputs of the MUX (I_0,I_1,I_2,I_3). **(7 points)**

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$I_0 = 0$
$I_1 = 1$
$I_2 = 1$
$I_3 = 0$



A B C
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1

I_3

11

Question#3] 15 points

Simplify using QM Tabulation method the following function

$$F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,10)$$

A B C D	
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
1 0 0 0	8
0 0 1 1	3
0 1 0 1	5
1 0 1 0	10
0 1 1 1	7

Table 1

	A B C D	
✓	(0,1) 0 0 0 -	
✓	(0,2) 0 0 - 0	
✓	(0,8) - 0 0 0	
✓	(1,3) 0 0 - 1	
✓	(1,5) 0 - 0 1	
✓	(2,3) 0 0 1 -	
✓	(2,10) - 0 1 0	
✓	(8,10) 1 0 - 0	
✓	(3,7) 0 - 1 1	
✓	(5,7) 0 1 - 1	

Table 2

	A B C D	
	(0,1,2,3) 0 0 - -	PI_1
	(0,2,1,3) 0 0 - -	///
	(0,2,8,10) - 0 - 0	PI_2
	(0,8,2,10) - 0 - 0	///
	(1,3,5,7) 0 - - 1	PI_3
	(1,5,3,7) 0 - - 1	///

Table 3

Table 4

	0	1	2	3	5	7	8	10
PI_1	x	x	x	x				
PI_2	x		x				x	(x)
PI_3				x		x	x	(x)

Essential

Essential

$$F = PI_3 + PI_2$$

answer??

13/15

Question#4] 20 points

A. Derive the truth table only of a combinational logic circuit which receives a 4-bit unsigned number **X** (X_3 X_2 X_1 X_0) as input and produces an output **Z** which equals the result of integer division of **X** by 3 (e.g., if **X**=7, **Z**=2). **10 points**

	X_0	X_1	X_2	X_3	Z_0	Z_1	Z_2	Z_3
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	0
3	0	0	1	1	0	0	0	1
4	0	1	0	0	0	0	0	1
5	0	1	0	1	0	0	0	1
6	0	1	1	0	0	0	1	0
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	1	0
9	1	0	0	1	0	0	1	1
10	1	0	1	0	0	0	1	1
11	1	0	1	1	0	0	1	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	1	0	0
14	1	1	1	0	0	1	0	0
15	1	1	1	1	0	1	0	1

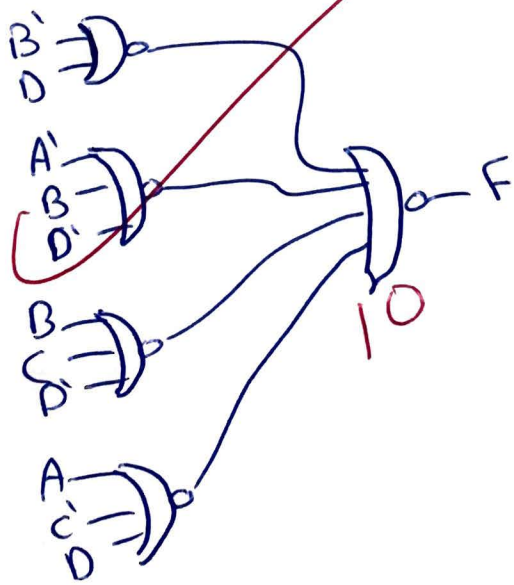
10

B. Implement the following function using NOR-NOR two level implementations
$F(A,B,C,D) = \sum (0,3,5,7,8,10,13,15)$ **10 points**

AB \ CD	00	01	11	10
00	1	0	1	0
01	0	1	1	0
11	0	1	1	0
10	1	0	0	1

mini
$F = B'C'D' + AB'D' + A'CD + BD$
0 00 100 011 11
Max

$(B'+D).(A'+B+D).(B+C+D').(A+C+D)$



3) module Wholesystem($I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, S_1, S_0, S_2, F$);

input [7:0] I;

input [2:0] S;

wire w_1, w_2;

output F;

~~Mux4x1 G1(I0, I1, I2, I3, S1, S0);~~

wire

~~G1(I0, I1, I2, I3, w1, S1, S0);~~

~~Mux4x1 G2(I4, I5, I6, I7, w2, S1, S0);~~

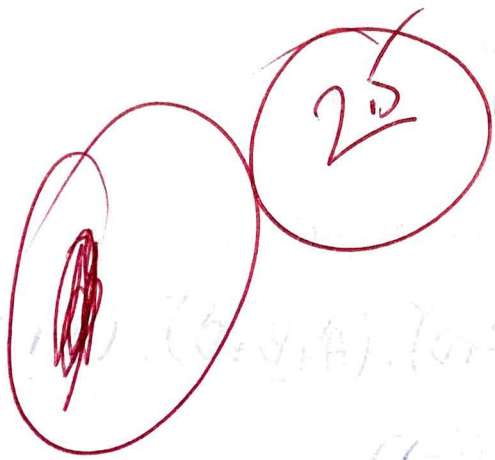
~~Mux2x1 G3(w1, w2, S2, F);~~

Mux4x1 $G_1(I_0, I_1, I_2, I_3, w_1, S_1, S_0)$;

Mux4x1 $G_2(I_4, I_5, I_6, I_7, w_2, S_1, S_0)$;

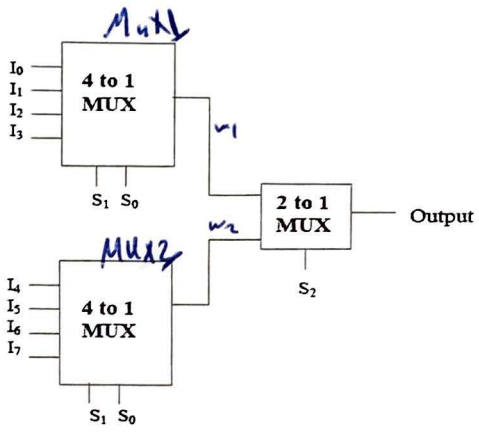
Mux2x1 $G_3(w_1, w_2, S_2, F)$;

endmodule



Question#5] 8 points

For the system shown in the following figure



00 —
01
10
11

1. **(2 points)** Write a Verilog HDL code to describe the module mux4×1
2. **(2 points)** Write a Verilog HDL code to describe the module mux2×1
3. **(4 points)** Write a Verilog HDL code to describe the whole system structurally from its subsystems

1)
```
module Mux4x1 (I0,I1,I2,I3,w1,S1,S0);
input I0,I1,I2,I3,S0,S1;
output w1;
wire w1;
assign w1=(!S1&&!S0)||(!S1&&S0)||(S1&&!S0)||(S1&&S0);
endmodule
```

2)
```
module Mux2X1(w1,w2,S2,F);
input w1,w2,S2;
output F;
assign if(S==0)
  F=w1;
else
  F=w2;
endmodule
```

على الصفحة السابقة