BIRZEIT UNIVERSITY

Electrical and Computer Engineering Department

Summer Semester 2019, Digital Systems (ENCS234), Second Exam

Time: 08:00 - 09:30   Date: 04/08/2019

Instructor: □ Ahmad Alsadeh   □ Aziz Qaroush

Student Name: ____________________________________ **Student ID**: ___________________

Question #	Full Mark	Student Mark
Q1	6	
Q2	6	
Q3	8	
Q4	12	
Q5	12	
Q6	6	
TOTAL	50	

Q1) (6 pts**):** Consider the following circuit constructed with a 4x1 multiplexor. Write the output function as sum of Minterms $\boldsymbol{F}(\boldsymbol{w},\boldsymbol{x},\boldsymbol{y},\boldsymbol{z}) = \sum(\ldots)$

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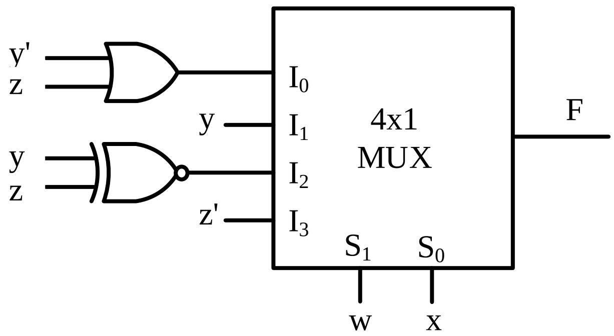
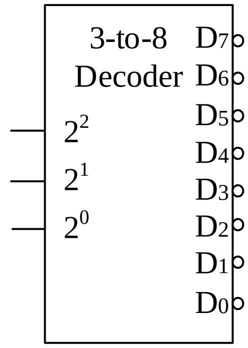
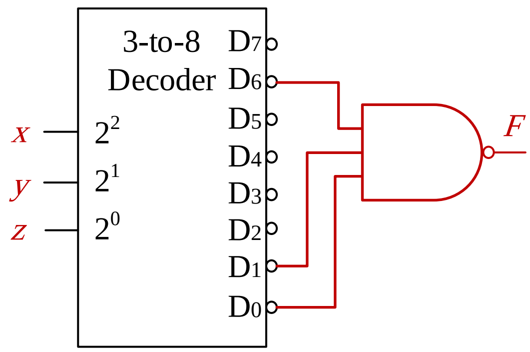


	w	*x*	*y*	*z*	*F*	
0	**0**	**0**	**0**	**0**	**1**	$I_0 = y' + z$
1	**0**	**0**	**0**	**1**	**1**	
2	**0**	**0**	**1**	**0**	**0**	
3	**0**	**0**	**1**	**1**	**1**	
4	**0**	**1**	**0**	**0**	**0**	$I_1 = y$
5	**0**	**1**	**0**	**1**	**0**	
6	**0**	**1**	**1**	**0**	**1**	
7	**0**	**1**	**1**	**1**	**1**	
8	**1**	**0**	**0**	**0**	**1**	$I_2 = y'z' + yz$
9	**1**	**0**	**0**	**1**	**0**	
10	**1**	**0**	**1**	**0**	**0**	
11	**1**	**0**	**1**	**1**	**1**	
12	**1**	**1**	**0**	**0**	**1**	$I_3 = z'$
13	**1**	**1**	**0**	**1**	**0**	
14	**1**	**1**	**1**	**0**	**1**	
15	**1**	**1**	**1**	**1**	**0**	

Q2) (6 pts**):** Design a circuit, which implements the function $F(x, y, z) = x'y' + xyz'$ using the following 3-to-8 decoder and minimum number of external gates.

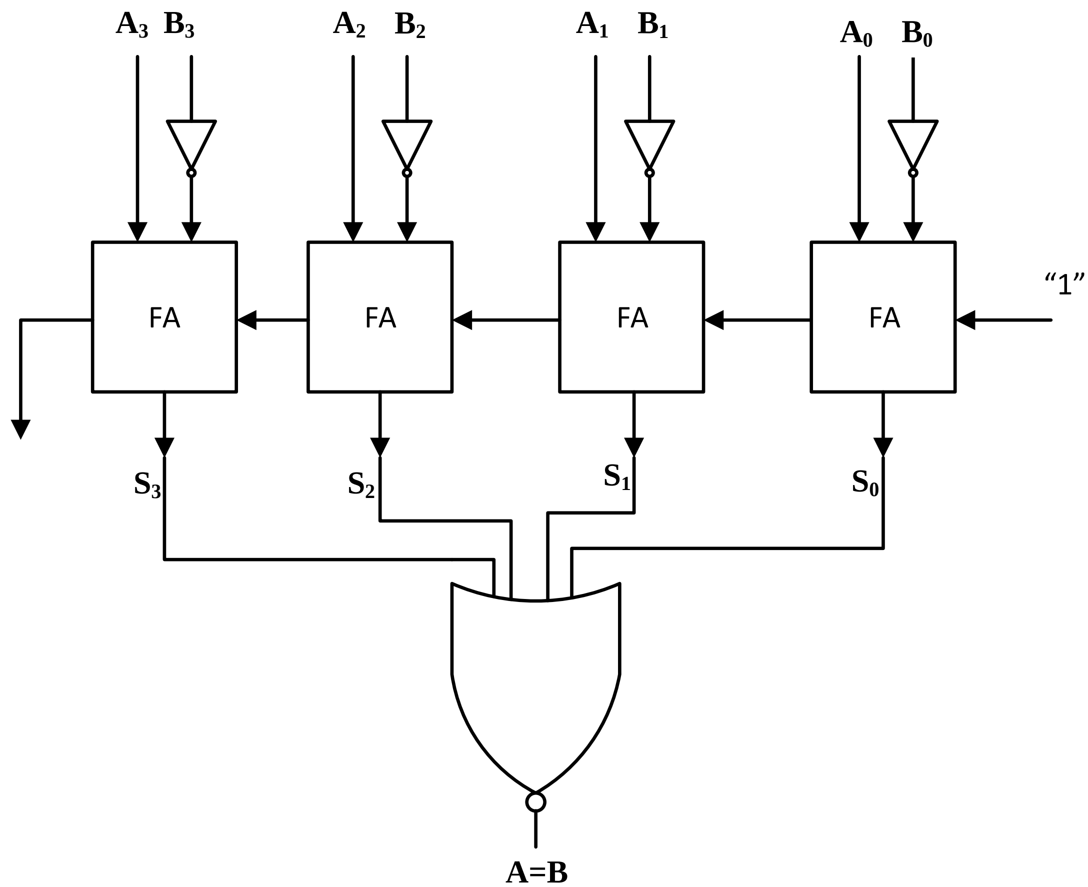


	x	***y***	***z***	***F***
0	**0**	**0**	**0**	**1**
1	**0**	**0**	**1**	**1**
2	**0**	**1**	**0**	**0**
3	**0**	**1**	**1**	**0**
4	**1**	**0**	**0**	**0**
5	**1**	**0**	**1**	**0**
6	**1**	**1**	**0**	**1**
7	**1**	**1**	**1**	**0**



$$F(x, y, z) = \sum(0, 1, 6,)$$

Q 3) (8 pts**):** With the addition of few logic gates, an *n*-bit ripple carry adder can be used to compare the magnitude of two n-bit unsigned numbers. For an input **$A=A_3A_2A_1A_0$** and **$B=B_3B_2B_1B_0$**, design a 4-bit digital circuit with appropriate logic gates and adder block diagrams with output *X* such that *X* is true when $A = B$. You may assume both **A** and **B** are unsigned numbers. Specify the value of any required control signals.



Q4 (12 pts) You are asked to implement a door security system by using a card reader. There are four inputs to the card reader: inputs *X*, *Y*, and *Z* are used to validate the correct door code, and input *V* is used to check if the card reader is still valid. After the card reader is being read by the system, there are three outputs to this system: alarm (*A*), door open (*D*), and Error (*E*). Door (*D*) will only open when the decimal value of the binary inputs (*X*, *Y*, *Z*) is odd AND the card reader is valid. The Error (*E*) signal goes on when the code on the card is correct (i.e. decimal value equal to odd) but the card is no longer valid. Finally, the alarm (*A*) will trigger when the code is incorrect.

a) Drive the truth table of this problem

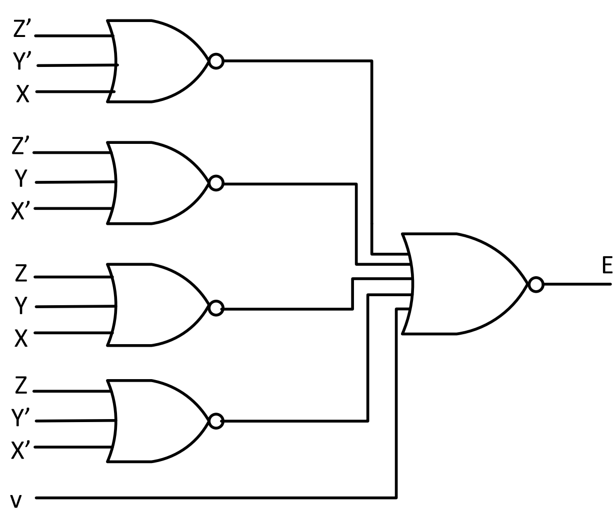
Inputs				**Outputs**		
X	***Y***	***Z***	***V***	***A***	***D***	***E***
0	0	0	0	1	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1
1	1	1	1	0	1	0

b) Use a Karnaugh map to find the reduced product-of-sum form of the Error (E) output**.**

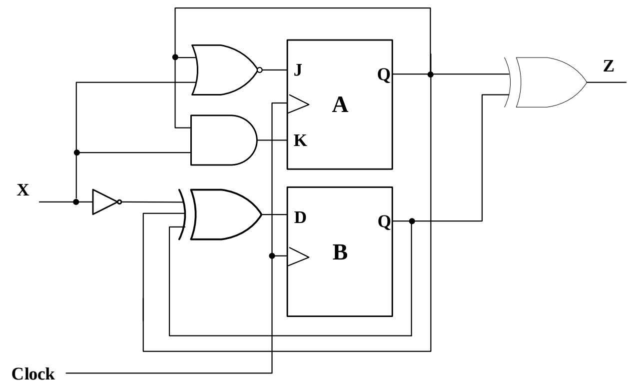
XY \ ZV	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	0	0	0	1
10	1	0	0	0

$$E = V'(X' + Y' + Z)(X + Y + Z)(X' + Y + Z')(X + Y' + Z')$$

c) Implement the Error (E) function circuit using two level NOR-NOR gates.



Q5) (12 pts) The sequential circuit shown below has a single output ***Z*** and input ***X***.



a) Derive expressions for the flip-flop inputs and the external output Z.

$J_A = (A + X)' = A'X', \qquad K_A = AX$

$D = A \oplus B \oplus X'$

$Z(t) = A \oplus B$

b) Write state equation for flip-flops

$$A(t+1) = J_A A' + K'_A A$$
$$A(t+1) = A'X'.A' + (AX)'A$$
$$A(t+1) = A'X' + (A' + X')A$$

$$A(t+1) = X'$$

$$B(t+1) = D_B = A \oplus B \oplus X'$$

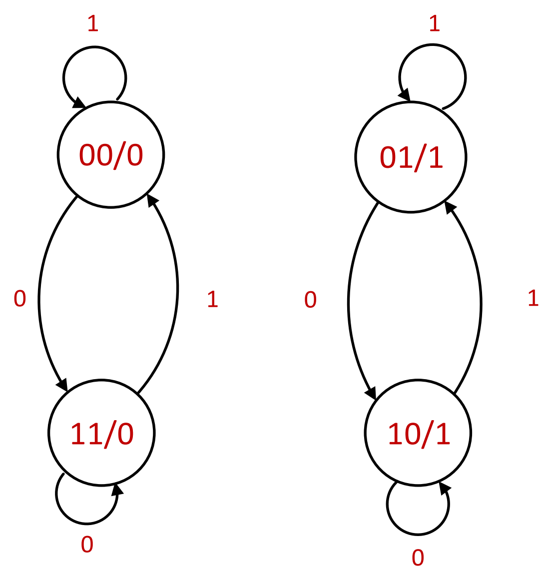
c) Derive the state table of the circuit

	Present State			*Next state*		*Output*
	A	***B***	***X***	***A***	***B***	***Z***
0	**0**	**0**	**0**	**1**	**1**	**0**
1	**0**	**0**	**1**	**0**	**0**	**0**
2	**0**	**1**	**0**	**1**	**0**	**1**
3	**0**	**1**	**1**	**0**	**1**	**1**
4	**1**	**0**	**0**	**1**	**0**	**1**
5	**1**	**0**	**1**	**0**	**1**	**1**
6	**1**	**1**	**0**	**1**	**1**	**0**
7	**1**	**1**	**1**	**0**	**0**	**0**

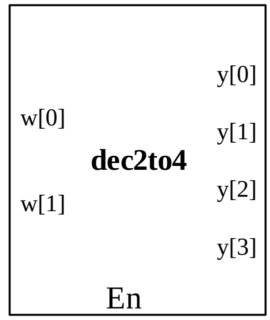
d) Is the circuit type Mealy or Moore? Why?

Moore machine .For the same state, the output does not change with the input

e) Draw the state diagram of the circuit.



Q6) (6 pts) Write a Verilog behavioral description for the module dec2to4




```
module dec2to4 (W, Y, En);
    input [1:0] W;
    input En;
    output [0:3] Y;
    reg [0:3] Y;

    always @(W or En)
        case ({En, W})
            3'b100: Y = 4'b1000;
            3'b101: Y = 4'b0100;
            3'b110: Y = 4'b0010;
            3'b111: Y = 4'b0001;
            default: Y = 4'b0000;
        endcase

endmodule
```