جامعة بيرزيت

**BIRZEIT UNIVERSITY**
**Faculty of Engineering and Technology**
**Electrical and Computer Engineering Department**

Summer Semester 2020/2021
Time: 16:15 - 17:15 (75 minutes)

Digital Systems (ENCS2340)

Second…Exam
Date: 22/08/2022

**Instructors:**

- ☐ Dr. Aziz Mohammed Qaroush - section 1
- ☐ Dr. Ayman Hroub - section 2
- ☑ Dr. Ayman Hroub - section 3
- ☐ Dr. Bilal Karaki - section 4

**Student Name:** yazan Abualown. **Student ID-:** 1210145

| Question # | Full Mark | Student's Mark |
|---|---|---|
| Q1 | 10 | 10 |
| Q2 | 7 | 6.5 |
| Q3 | 8 | 7.5 |
| TOTAL | 25 | 24 |

**Question 1**: (**60 points**, 3 points each). Select the correct answer

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|
| C ✓ | D ✓ | B ✓ | B ✓ | A ✓ | C ✓ | C ✓ | C ✓ | D ✓ | D ✓ |

…

1- We can construct a 5-to-32-line decoder using:

A- Five 2-to-4-line decoders with enable.
B- Two 4-to-16-line decoders without enable and NOT-gate.
C- Four 3-to-8-line decoders with enable and a 2-to- 4-line decoder.
D- Nine 2-to-4-line decoders with enable.

2- Consider a J-K flip-flop. Let the present state Q=0, J=1, and K=1, what will be the next state Q after one clock?

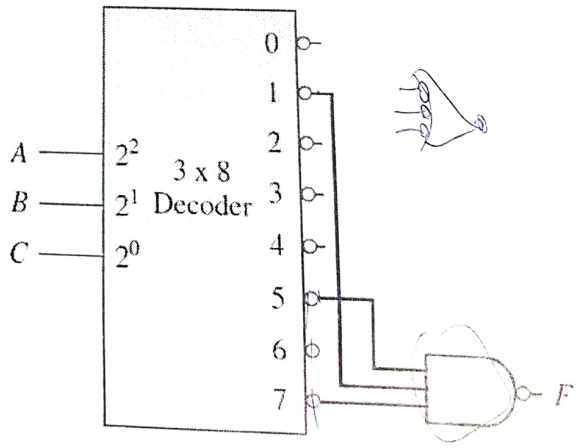
A. Open circuit (High Impedance)
B. Q=2
C. Q=0
D. Q=1
E. None of the above.

3 - A digital circuit has two inputs X & Y each has a 2-bit unsigned number. Its output Z is the multiplication of the given inputs Z=X*Y. The minimum number of bits required for the output number Z is

A- 3
B- 4
C- 5
D- 6

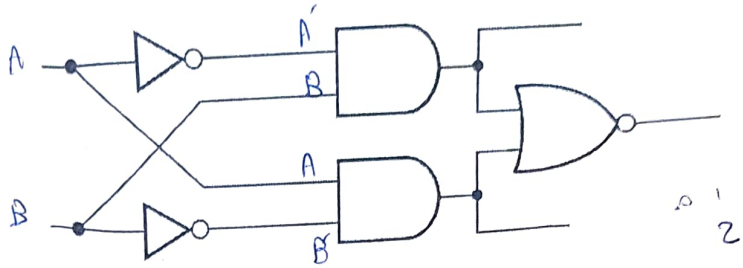
4- The following circuit is an implementation for

A. F(A, B, C) = ∑m (0, 1, 3, 4 )
B. F(A, B, C) = ∑ m(1,5,7 )
C. F(A, B, C) = ∑ m(0,1,5,7 )
D. F(A,B,C) =∑m (0, 2, 3, 4, 7)
E. None



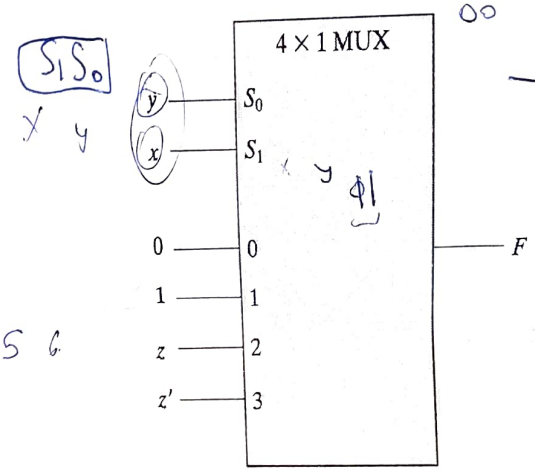
5- The following circuit is an implementation of:

A- One bit comparator.
B- R-S Latch.
C- D-Flip-Flop.
D- D-Latch.
E- Non of the above.




6- What is the Boolean function F(x,y,z) that is implemented with a 4 x 1 multiplexer as shown below.

A- $F(x,y,z) = \sum (0, 1,5,6)$
B- $F(x,y,z) = \sum (2, 3,4,7)$
C- $F(x,y,z) = \sum (2, 3,5,6)$
D- $F(x,y,z) = \sum (0,1,4,7)$
E- None of the above

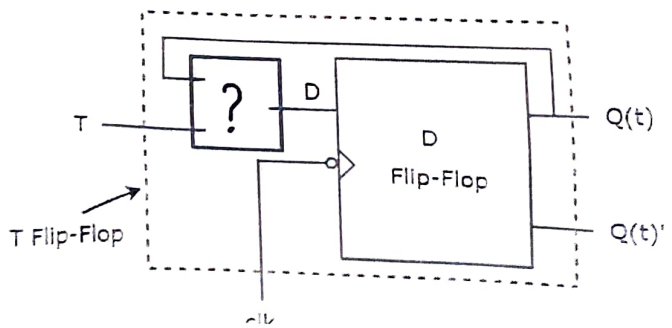



7- The implementation of a full adder can be implemented using two half adders and

A- Priority encoder
B- NAND gate
C- OR gate
D- NOR gate
E- AND gate

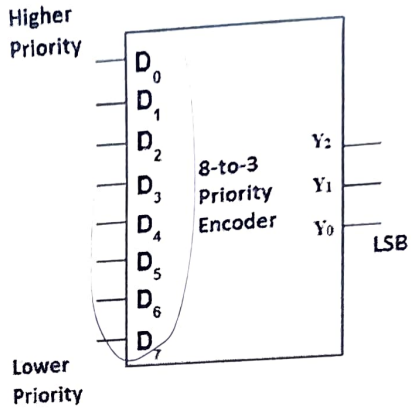
8- To construct a T-flip-flop using D-flip-flop as shown below, we need to use

A- Not gate.
B- AND gate.
C- XOR gate.
D- XNOR gate.
E- OR gate.



9- In the priority encoder shown with $D_0$ having highest priority and $D_7$ the lowest priority, if the status at inputs $D_3 = 1$ and $D_7 = 1$ and all other inputs are set to zero then the output of the encoder is

A. $Y_2 = 1$, $Y_1 = 1$, and $Y_0 = 0$.
B. $Y_2 = 1$, $Y_1 = 1$, and $Y_0 = 1$.
C. $Y_2 = 0$, $Y_1 = 0$, and $Y_0 = 1$.
D. $Y_2 = 0$, $Y_1 = 1$, and $Y_0 = 1$.
E. None




10- Consider the following Verilog module:

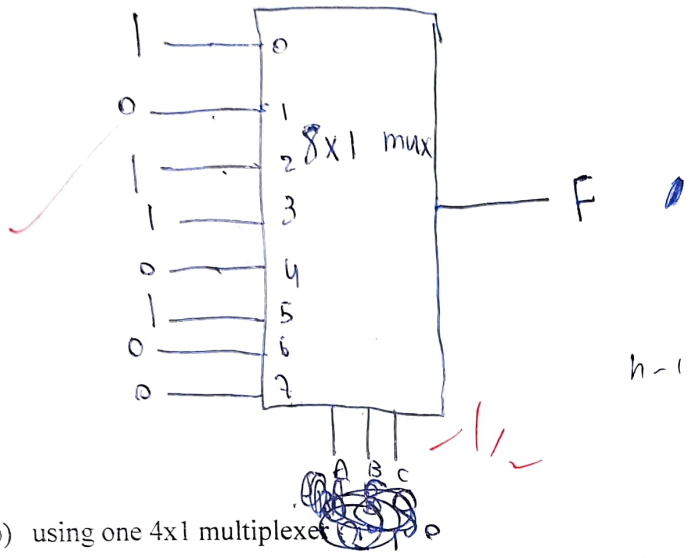
```
module sec1234(A,B,C);

 input A, B;
 output C;
 wire notA, notB, w1, w2;

not  G1(notA, A);
not  G2(notB, B);
and  G3(w1, A, notB);
and  G4(w2, B, notA);
or   G5(C, w1, w2);

endmodule
```

This module can be used as an alternative to:

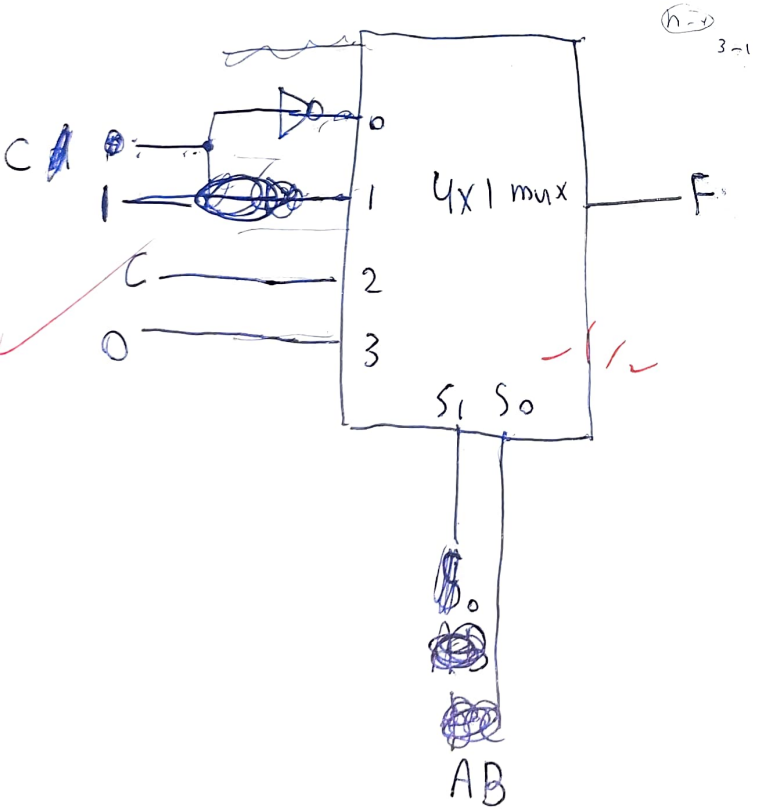
A. Decoder
B. MUX
C. XNOR gate
D. XOR gate
E. None of the above

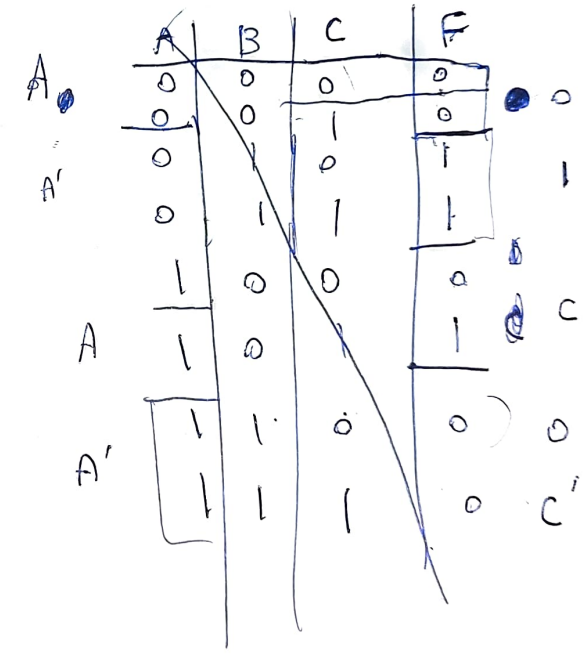
Q 2) Implement the Boolean function $F(A,B,C) = \sum m(0,2,3,5)$

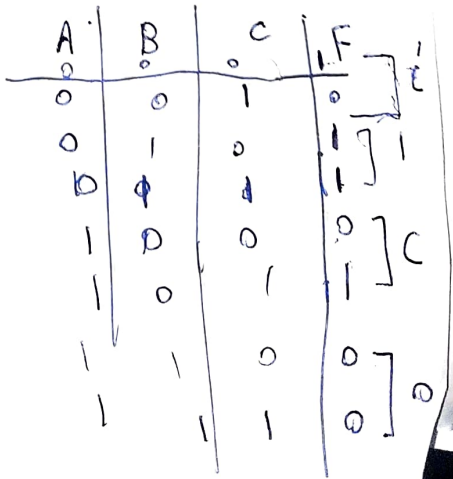
a) using one 8x1 multiplexer

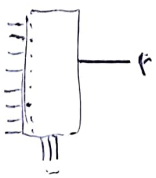



b) using one 4x1 multiplexer



7 8

Q 3) Design a combinational logic circuit that receives a 3-bit unsigned number X and produces the floor of $\frac{X}{2}$, i.e. $Z = \left\lfloor \frac{X}{2} \right\rfloor$. (e.g. if X=5 then $Z = \left\lfloor \frac{5}{2} \right\rfloor = \lfloor 2.5 \rfloor = 2$).

| $X_2$ | $X_1$ | $X_0$ | $R_2$ | $R_1$ | $R_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |

$R_2 = 0$

$R_1$

| $X_2$ \ $X_1X_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| $X_2$ | | | | |
| $X_2'$ | 1 | 1 | 1 | 1 |

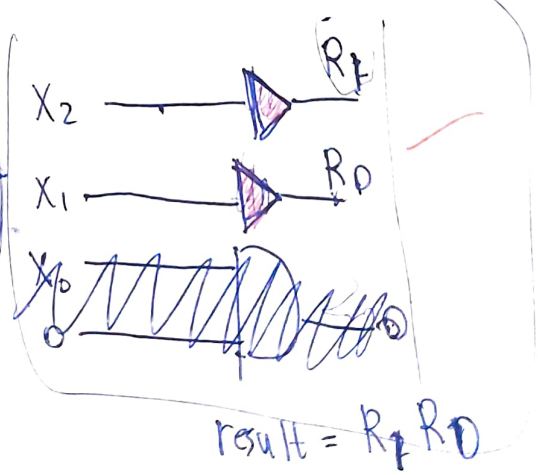
$R_1 = X_2$

MSB

$R_0 = X_1$

LSB

| $X_2$ \ $X_1X_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | 1 | 1 |
| 1 | | | 1 | 1 |


result = $R_1 R_0$