Digital Design HDL Homework

ENCS234

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Section# : 1

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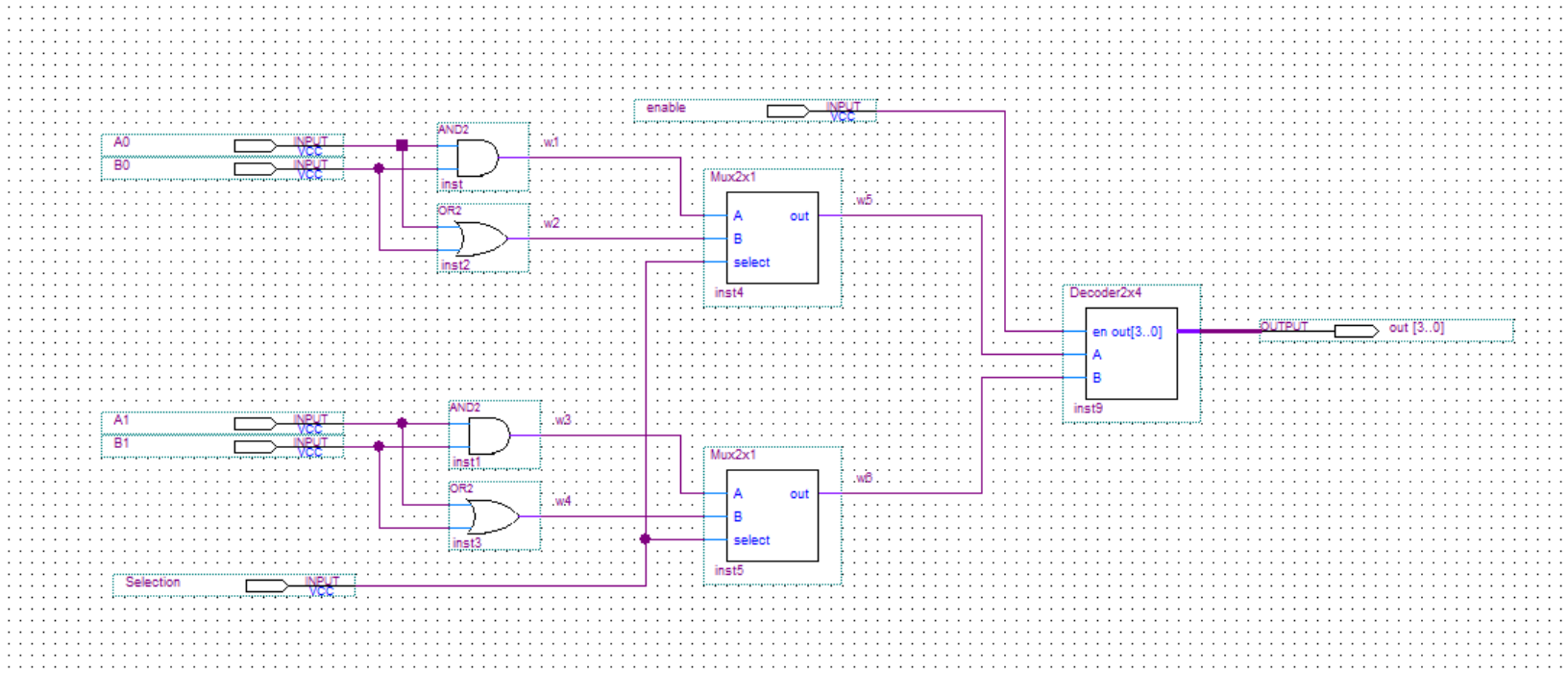
1 - Verilog HDL code to describe the module mux2×1 :

```
1  module Mux2x1(A,B,select,out);
2    input A,B,select;
3    output out;
4    reg out;
5    always @(select)
6    if (select ==1)
7    out = A;
8    else
9    out = B;
10   endmodule
```

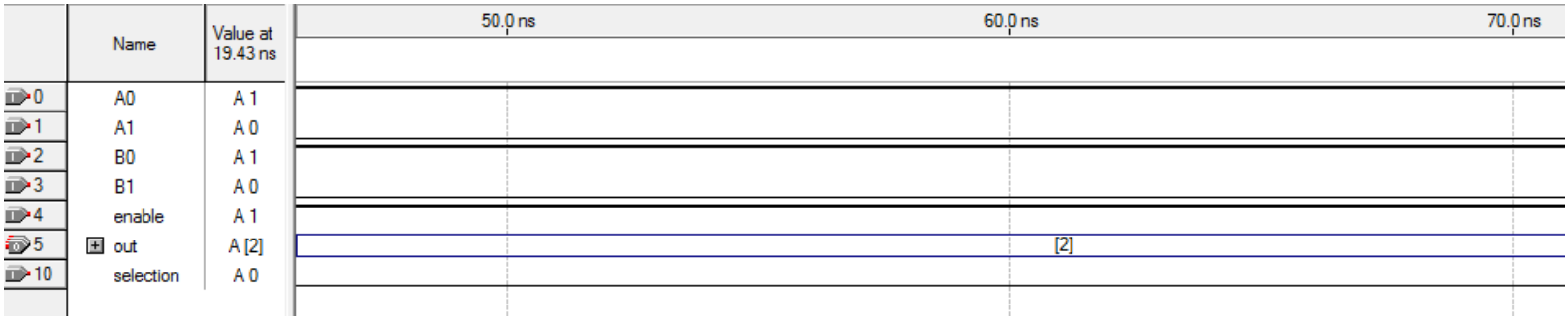
2 - Verilog HDL code to describe the module dcdr2×4 :

```
1  module Decoder2x4 (en,A, B,out);
2  input A, B;
3  input en;
4  output[3:0] out ;
5  reg [3:0] out ;
6  initial
7  out = 4'b0000;
8  always
9  begin
10 if(en)
11 begin
12 if(A ==0 && B ==0)
13   out = 4'b1000;
14   else if( A ==0 && B==1)
15       out = 4'b0100;
16       else if( A==1 && B==0)
17          out = 4'b0010;
18          else
19            out = 4'b0001;
20    end
21    end
22 endmodule
```

3 - Block Diagram :



Block diagram simulation :



4 - Verilog HDL code to describe the whole system structurally from its subsystems :

```
1  module HDLHW (A0, A1, B0, B1 , out , selection , enable);
2  input A0, A1, B0, B1, selection, enable;
3  output [3:0] out;
4  wire w1,w2,w3,w4,w5,w6;
5
6
7   assign w1=(A0&&B0);
8   assign w2=(A0||B0);
9   and G1(w3,A1,B1);
10  or G2(w4,A1,B1);
11  Mux2x1 m1(w1,w2,selection,w5);
12  Mux2x1 m2(w3,w4,selection, w6);
13  Decoder2x4 D1(enable, w5, w6, out);
14
15
16  endmodule
```

simulation :