ENCS 234 – Digital Systems – First Semester 2015/2016

Homework set 4

Issued Monday 21-12-2015

Due Monday 4-1-2016 for sections 1, 2, and 5 (Beginning of class)

Due Tuesday 5-1-2016 for sections 3 and 4 (Beginning of class)

This homework covers chapter 5 and sections 6.1 and 6.2

Problem 1:

A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.
(b) Derive the characteristic equation.
(c) Tabulate the excitation table.
(d) Show how the PN flip-flop can be converted to a D flip-flop.

Problem 2:

A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$J_A = x$ $K_A = Bx$ $J_B = x' + A$ $K_B = A' + B$

(a) Derive the state equations A(t + 1) and B(t + 1),
(b) Draw the state diagram of the circuit.

Problem 3:

For the following state table:

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Draw the corresponding state diagram.

(b) For the input sequence 01110010011, determine the output sequence.
(c) Reduce this state machine using the Implication Table method.
(d) Draw the state diagram for the reduced state table.
(e) For the input sequence 01110010011, determine the output sequence using the reduced state machine. Verify that you get the same output sequence as that in part b.
(f) Using a binary state assignment (a=00, b=01, …) and JK flip-flops, design a sequential circuit that implements the reduced state machine you found in part c.

Problem 4:

Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and its 2's complement shifted into the other side of the shift register.