

# **Digital Project**

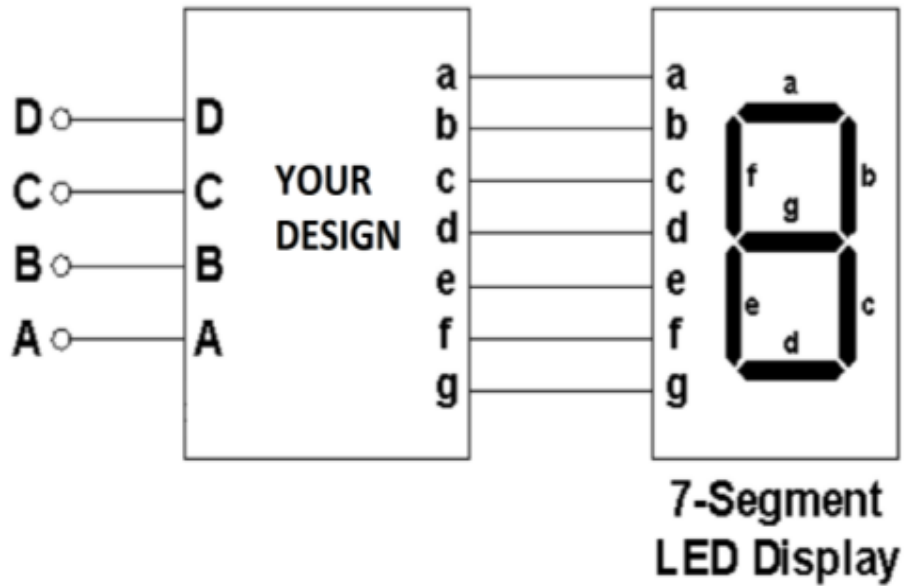
**Name : Samer Demaidi**

**ID : 1131785**

**Section : 1**

## Description :

Design a combinational circuit using Verilog to achieve the following functionality.



Your system will have 4 inputs (A, B, C, D) and 7 outputs (a through g) that drive a 7-segment display, whose inputs are active-high. The system shall behave according to the following table:

A	B	C	D	Display
0				The least significant decimal digit of your student ID
1				The second least significant decimal digit of your student ID
2				The third least significant decimal digit of your student ID
3				The fourth least significant decimal digit of your student ID
4				The fifth least significant decimal digit of your student ID
5				The sixth least significant decimal digit of your student ID
6				The most significant decimal digit of your student ID
7				The least significant decimal digit of your birth year
8				The second least significant decimal digit of your birth year
9				The third least significant decimal digit of your birth year
10				The most significant decimal digit of your birth year
11 - 15				Nothing

## Design :

### 1) Code:

```
module samer_7_segmentDesign(a,b,c,d,A,B,C,D,E,F,G);  
  
input a,b,c,d; //inputs  
  
output A,B,C,D,E,F,G; //outputs  
  
  
assign A=(!b && !c) || (!a && !c && !d) || (!a && !b && !d) || (!a &&  
b && c && d) ; //equation of output A  
  
assign B=(a &&!b && !c) || (!b && !c && d) || (!a && !b&& c && !d )  
|| (!a && b && !c && !d) ;//equation of output B  
  
assign C=(!b && !c) || (!a && !c && !d) || (!a && !b && !d) || (!a && b  
&& c && d) ; //equation of output C  
  
assign D=(!b && !c) || (!a && !c && !d) || (!a && b && c && d )  
; //equation of output D  
  
assign E=(!a && !b && d) || (!a && !c && d) || (!a && b && c && !d )  
|| (a && !b && c && !d) ; //equation of output E  
  
assign F=(!a && d) || (!b && !c) || (!a && b && c) || (a && !b && !d )  
; //equation of output F  
  
assign G=(!b && !c) || (!a && !c && !d) || (!a && b && c && d )  
; //equation of output G  
  
  
//outputs will be obtained from those equations  
  
endmodule
```

2) simulation to show that the code works well :

