DIGITAL PROJECT

ENCS234

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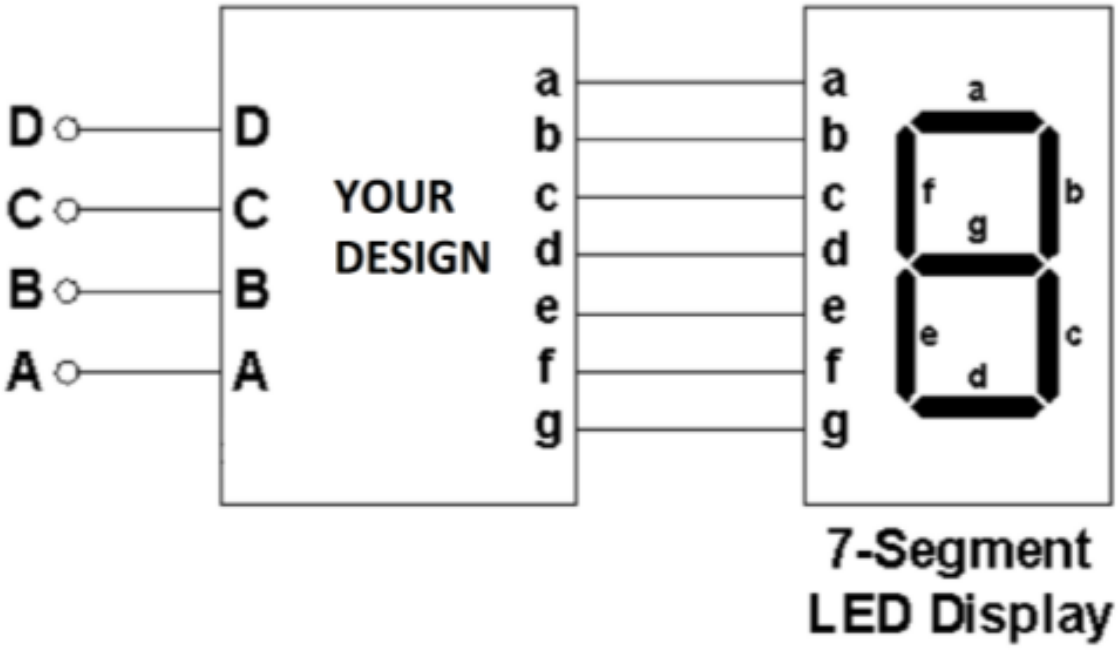
ID# : 1140427

Section : 1

D.Abdel salam sayaad

١.Description :

Design a combinational circuit using Verilog to achieve the following functionality.



Your system will have 4 inputs (A, B, C, D) and 7 outputs (a through g) that drive a 7-segment display, whose inputs are active-high. The system shall behave according to the following table:

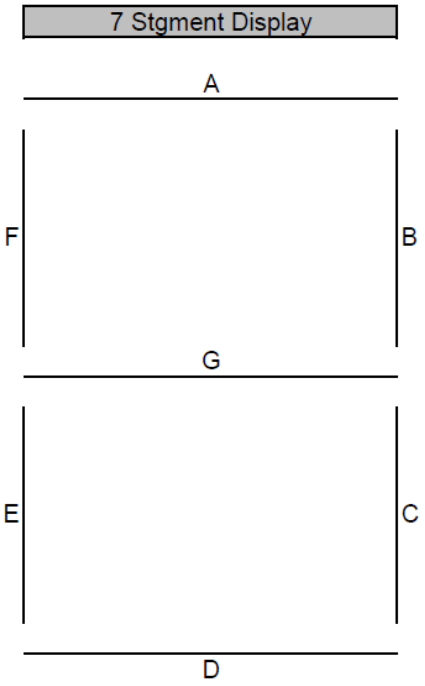
A B C D	Display
0	The least significant decimal digit of your student ID
1	The second least significant decimal digit of your student ID
2	The third least significant decimal digit of your student ID
3	The fourth least significant decimal digit of your student ID
4	The fifth least significant decimal digit of your student ID
5	The sixth least significant decimal digit of your student ID
6	The most significant decimal digit of your student ID
7	The least significant decimal digit of your birth year
8	The second least significant decimal digit of your birth year
9	The third least significant decimal digit of your birth year
10	The most significant decimal digit of your birth year
11 - 15	Nothing

2.My Design

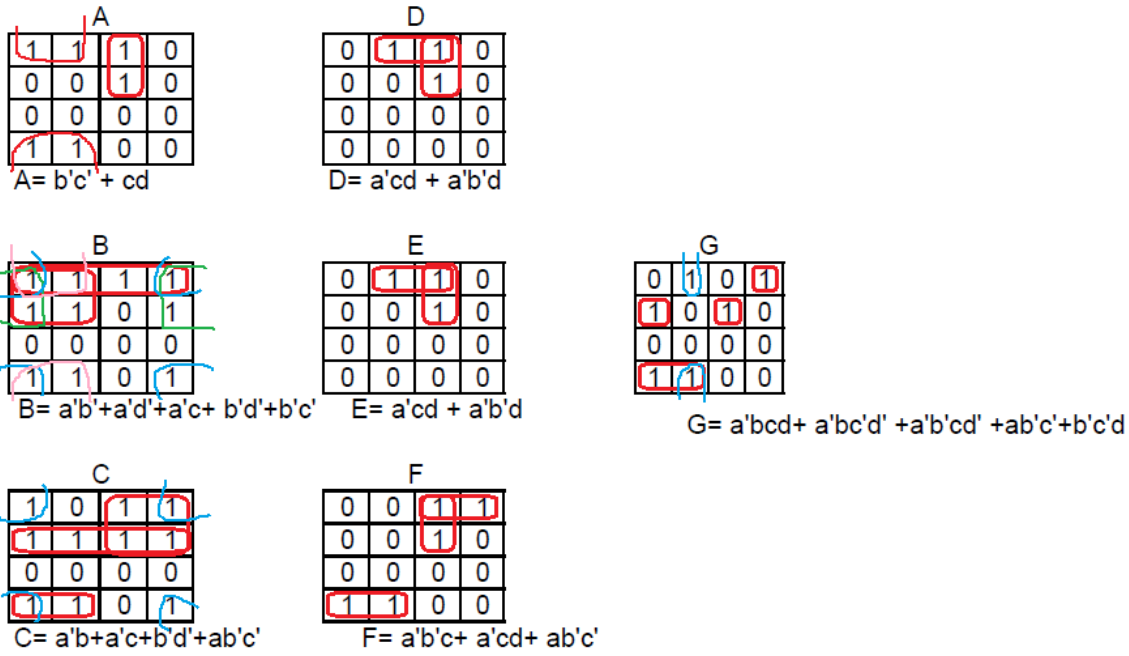
i.Truth Table

ID#	1140427
Birth Year	1996

	Inputs	Outputs
Input > Output	a b c d	A B C D E F G
0 > 7	0 0 0 0	1 1 1 1 0 0 0
1 > 2	0 0 0 1	1 1 0 1 1 0 1
2 > 4	0 0 1 0	0 1 1 0 0 1 1
3 > 0	0 0 1 1	1 1 1 1 1 1 0
4 > 4	0 1 0 0	0 1 1 0 0 1 1
5 > 1	0 1 0 1	0 1 1 0 0 0 0
6 > 1	0 1 1 0	0 1 1 0 0 0 0
7 > 6	0 1 1 1	1 0 1 1 1 1 1
8 > 9	1 0 0 0	1 1 1 0 0 1 1
9 > 9	1 0 0 1	1 1 1 0 0 1 1
10 > 1	1 0 1 0	0 1 1 0 0 0 0
11-15 > nothing	x x x x	0 0 0 0 0 0 0



ii.k-maps



iii. Code :

```
module maryam_1140427(a,b,c,d,A,B,C,D,E,F,G);
input a,b,c,d; // inputs
output A,B,C,D,E,F,G; // outputs
/*
 A,B,C,D,E,F,G are equations for optainig the outputs :
*/
assign A=  ( !b && !c )||(!a && c && d); // the equasion of A
assign B=  ( !a && !b ) ||  ( !b && !d ) || ( !a && !d ) || (!a && !c) || (!b && !c); // the equasion of B
assign C=  ( !a && b) || (!a && c) || ( !b && !d ) || (a && !b && !c); // the equasion of C
assign D=  ( !a && c && d) || ( !a && !b && d ); // the equasion of D
assign E=  ( !a && c && d) || ( !a && !b && d ); // the equasion of E
assign F=  ( !a && !b && c )|| (!a && c && d ) || ( !a && !b && !c ); // the equasion of F
assign G=  ( !a && b && c && d) || ( !a && b && !c && !d ) || ( !a && !b && c && !d )||
           ( a && !b && !c)||(!b && !c && d) ; // the equasion of G
endmodule
```

iv.Simulation: