BIRZEIT UNIVERSITY

Department of Electrical and Computer Engineering
Summer Semester, 2019/2020

Digital Systems - ENCS234

Verilog Assignment

Groups*: At most two students can form a group*

Problem: Design and Simulation of 8-bit ALU

Design an 8-bit ALU circuit that receives two 8-bit input numbers `X[7:0]` and `Y[7:0]`, and produces a 8-bit output `Z[7:0]`, an output carry `Cout`, an overflow flag `OV`, and `Zero` flag. The circuit implements the following 12 functions based on a 3-bit control input `C[3:0]`:

Code	Function
000	Addition: `Z=X+Y`
001	Subtraction: `Z=X-Y`
010	Reminder: `Z=X%Y`
011	Bitwise AND: `Z=X&Y`
100	Bitwise OR: `Z=X|Y`
101	Concatenate: `Z={X[3:0] , Y[3:0]}`
110	Equality: Zero=`X==Y`
111	Less than: `Cout=X<Y`

Notes:

a) Show the block diagram design of your 8-bit ALU using components like Adder, Multiplexor, etc. as needed.
b) Model each component separately. You should have different modules for the adder, multiplexer, etc.
c) Write a Verilog test scenarios to test both the 8-bit ALU. Verify the correctness by simulation.
d) Show snapshots of all simulation waveforms.
e) Submit a report (Word or PDF document) should contain Problem description, the block diagram, a copy of the Verilog modules and the waveforms taken directly as snapshots from the simulator.

Deadline: 26\8 Submission of soft copy (code + report)