BIRZEIT UNIVERSITY

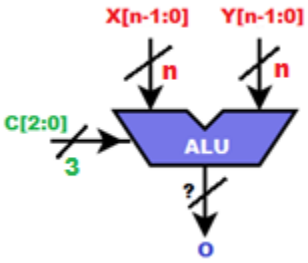
First Semester, 2022/2023

Digital Systems ENCS234 – **Verilog Project**

Problem: Modeling a Multifunction ALU

Design and implement a multifunction arithmetic and logic unit (ALU) based on the following specifications:

1. **X** and **Y** are the inputs of the unit and they are n-bit signed numbers represented in 2's complement.
2. **C** is a 3-bit unsigned number and used to select the operation of the unit (i.e. arithmetic or logical operation).
3. **O** is the signed ALU output and represented in 2's complement. Note that, you are required to define the minimum number of bits needed for **O** that will make the overflow never occurs in this design.
4. ALU symbol and the supported functions are represented as follow:

ALU Function Code (C)	ALU Output (O)	ALU Symbol
000	(**X**+**Y**)/2	
001	2*(**X**+**Y**)	
010	(**X**/2)+**Y**	
011	**X**-(**Y**/2)	
100	**X** NAND **Y**	
101	NOT(**X**)	
110	**X** NOR **Y**	
111	**X** XOR **Y**	

Based on the above specifications, answer the following points:

a) (**5 points**) Specify the size of the output (**O)** in bits so the overflow can never occur.

b) (**10 points**) Show the ALU implementation using medium-scale integration (MSI) components and minimum number of gates (i.e. in blocks with their sizes). Note that, you might use some kind of extension (sign- or zero-extension).

c) (**10 points**) Write behavioral Verilog modules for your elements you defined in Part (b). Be noted that the size of every element you define should be **parameterized**, so that you can vary the design during the testing phase.

d) (**5 points**) Write a structural Verilog model for your ALU designed in Part (b) using the elements you defined in Part (c).

e) (**5 points**) Generate the waveforms of the ALU defined in Part (d), assumes that X and Y are 4-bits and their values based on your student ID should be set as follows:

The general representation of the student ID is **$1C_2Y_2X_2C_1Y_1X_1$**, so, if your student ID is 1220520, then X, Y, and C values for the three test cases as follows:

Test	X	Y	C	O
1	$X_1 = 0$	$Y_1 = 2$	$C_1 = 5$	NOT(**0**)
2	$X_2 = 0$	$Y_2 = 2$	$C_2 = 2$	((**0**)/2)+(**2**)
3	$X_3 = -X_1$	$Y_3 = -Y_1$	$C_3 = C_2$	((**0**)/2)+(**-2**)

Note: If any value from the set {C_2, Y_2, X_2, C_1, Y_1, X_1} is 8 or 9, you need to replace it by 1

f) (**10 points**) Write a single behavioral Verilog module that models the designed ALU.

g) (**5 points**) Generate the waveforms of the behavioral ALU defined in Part (f), assumes that X and Y are 4-bits and their values based on your student ID should be set as follows:

The general representation of the student ID is **$1C_2Y_2X_2C_1Y_1X_1$**, so, if your student ID is 1220520, then X, Y, and C values for the three test cases as follows:

Test	X	Y	C	O
1	$X_1 = 0$	$Y_1 = 2$	$C_1 = 5$	NOT(**0**)
2	$X_2 = 0$	$Y_2 = 2$	$C_2 = 2$	((**0**)/2)+(**2**)
3	$X_3 = -X_1$	$Y_3 = -Y_1$	$C_3 = C_2$	((**0**)/2)+(**-2**)

Note: If any value from the set {C_2, Y_2, X_2, C_1, Y_1, X_1} is 8 or 9, you need to replace it by 1

Instructions:

1. This project is to be done individually.
2. This project should be implemented in **Verilog HDL** using **Quartus** software.
3. Snapshots should be clear and should contain the date and the time of your computer.
4. Captions should be added to your figures and tables. Also, you are required to explain and describe these figures and tables in your project.
5. Comments are required to be added in your Verilog codes.

Submission:

You are required to submit a compressed file (**.zip file**) and it should contain:

a. Project folder, name it by "**Project_ID**" (if your ID is 1220520, then the folder name should be "**Project_1220520**"). This folder should contain all modules files (i.e. Verilog files and Waveforms), name your modules/waveforms by *moduleName*_ID and *waveformName*_ID (e.g. if your module is Adder and your ID is 1191020, then the name of the module should be "**Adder_1220520**").

b. Report in **pdf** format (only pdf format), name it by "**Report_ID**" (if your ID is 1220520, then the folder name should be "**Report_1220520**"**.** This report should contain your answers for all parts with detailed explanation and supported by snapshots/figures**,** commands, designs, runs, tables, etc.