جامعة بيرزيت
BIRZEIT UNIVERSITY

Computer Organization and architecture (ENCS238)
Midterm Exam

Spring semester 2014/2015 Date: 26/3/2015
Instructors: Dr. Abualsoud Hanani
Dr. Hanna Bullata Time allowed: 90 minutes

Name: Key ID: .

⇨ **Circle your section: sec 1 (SMW 9-10), Sec 2 (SMW 11-12), Sec 3 (SMW 12-1)**

Instructions:

- **You have 90 minutes (1.5 hours), budget your time carefully!**
- **Turn off your mobile.**
- **To make sure you receive credit, please write clearly and show your work.**

Question	Maximum	Mark	ABET SO
1	16		
2	12		A
3	10		C
4	16		A
5	6		E
Total	60		

Question 1 (15 marks)

1. Virtually all computer designs are based on the von Neumann architecture. A high level view of this architecture has the following three components:
   (A) Buses, memory, input/output controllers (B) Hard disks, floppy disks, and the CPU
   (C) Memory, the CPU, and printers (D) memory, input/output modules, and the CPU

2. Which of the following languages a program is written in can be executed by a CPU directly?
   (A) C (B) C++
   (C) Assembly (D) Machine language
   (E) None of the above

3. When perform $(10000111)_2$ - $(11001000)_2$, how will the Condition Code bits be set.
   (A) CF=0, OF=0 **(B)** CF=1, OF=0
   (C) CF=0, OF=1 **(D)** CF=1, OF=1

4. Computers use addressing mode techniques for _____.
(A) Giving programming versatility to the user by providing facilities as pointers to memory counters for loop control

(B) Reducing number of bits in the field of instruction

(C) Specifying rules for modifying or interpreting address field of the instruction

(D) All the above

5. In IEEE 754 single precision, the maximum absolute number that can be represented is (approximately):
(A) 3.4x10^38 (B) 2x2^128
(C) 1x2^127 (D) 2x10^34

6. A Stack-organized Computer uses instruction of
(A) Indirect addressing (B) Two-addressing

(C) Zero addressing (D) Index addressing

7. 1MB (one Mega Bytes) is
(A) 10^6 bytes (B) 2^30 bytes
(C) 10^20 bytes (D) 2^20 bytes
(E) None of the above

8. The operation executed on data stored in registers is called
(A) Macro-operation (B) Micro-operation

(C) Bit-operation (D) Byte-operation

9. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called
(A) Data transfer instructions. (B) Program control instructions.

(C) Input-output instructions. (D) Logical instructions.

10. A computer's memory is composed of 4K words of 16 bits each. How many bits are required for memory address if smallest addressable unit is one word?
(A) 13 (B) 12
(C) 10 (D) 5

11. Programs are transferred into the CPU for execution directly from
(A) Keyboard (B) Cache
(C) Hard drives (D) Main memory
(E) None of the above

12. There is no underflow in integer calculations.
(A) True (B) False

13. CISC machines provide the programmer with fewer instructions than RISC machine.
(A) True (B) False

14. Every bit in the memory of a computer has an address
(A) True (B) False

15. What is the most positive value that can be stored using 10-bit unsigned binary representation?
(A) 2^{11} (B) $2^{11} - 1$ (C) 2^{10} (D) $2^{10} - 1$ (E) 2^9 (F) $2^9 - 1$

16. A computer system has Five 4-bit registers. We need to implement a shared 8-bit data bus. We need:
A) Four 8x1 multiplexers
B) Eight 4x1 multiplexers
C) Five 4x1 multiplexers
D) Eight 2x4 decoders
E) Eight 8x1 multiplexers

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
D	D	A	D	A	C	D	B	A	B	D	A	B	B	D	A

Question 2 (12 points)

a) Use Booth's algorithm to find the result of multiplying (8) by (-5). Clearly show all steps and verify your final answer. [10pts] needs a min. of 5 bits {each step 2 pts}.

A	Q	Q-1	M	Comments
00000	01000	0	11011	Initial values
00000	00100	0	11011	SAR 1
00000	00010	0	11011	SAR 2
00000	00001	0	11011	SAR 3
00101	00001	0	11011	Sub } 4
00010	10000	1	11011	SAR }
11101	10000	1	11011	ADD } 5
11110	11000	0	11011	SAR }
Result = -40				

b) How many addition and how many subtraction operations are needed when using Booth's algorithm to multiply a number X by the multiplier "00110110100" [2pts]

Σ1 Number of Addition Operations: 3

Σ1 Number of Subtraction Operations: 3

Question 3 (10 points)

A Digital computer has a memory unit with 32 bits per word (memory element). The instruction set consists of 260 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.

a) How many bits are needed for the opcode?

(2.5) 9 bits

b) How many bits are left for the address part of the instruction?

(2.5) $32 - 9 = 23$ bits

c) What is the maximum allowable size for memory that can be accessed directly?

(2.5) $2^{23} W = 2^{23} \times 4$ bytes $= 2^{25} = 32M$ bytes

d) What is the largest signed binary number that can be accommodated in one word of memory?

(2.5) $2^{31} - 1$

Question 4 (16 points):

a) Consider a 16-bit floating-point format given in Figure below: [8pts]

Sign=1bit	Exponent=7bits	Significant=8bits

Let x = (AB12)H is floating-point number, expressed in hexadecimal. Find the representation of x in 16-bit format given above (show how the floating point calculations are performed step by step).

1 0101011, 00010010

s exp sig

$= -1.00010010 \times 2^{-20}$

Bias $= 2^6 - 1 = 63$

exp $= 43 - 63 = -20$

b) Show the value represented by **10101100** (binary) if it is [8pts]

(2) (a) Sign magnitude -44

(2) (b) One's complement -83

(2) (c) Two's complement

(2) (d) Biased (Excess) -84

Bias $= 127$

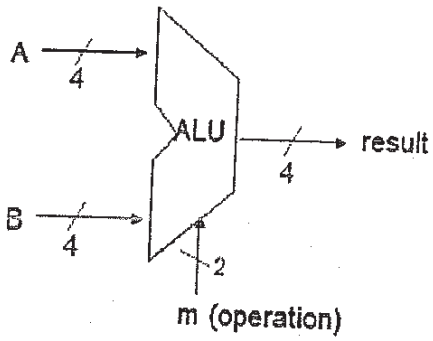
$(10101100)_2 = 172$

Value $= 172 - 127 = 45$

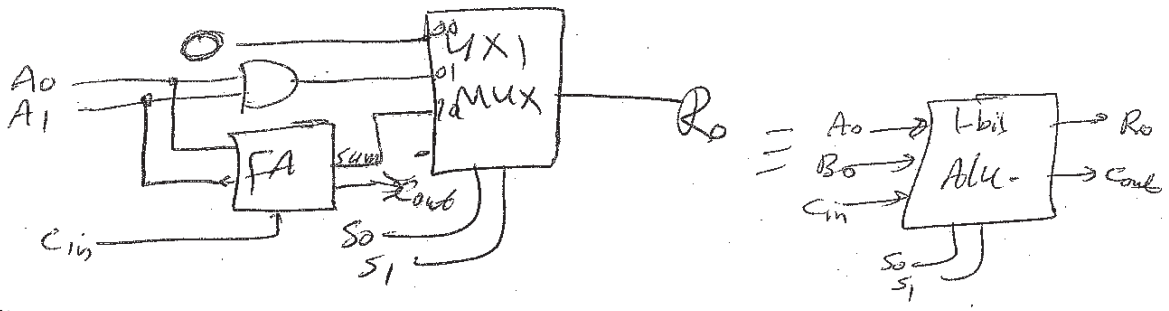
Question 5 (6 points)

It is required to design a 4-bit ALU that can perform the operations specified in the following table. This ALU has the interface specified to the right.

Operation	Function
00	Logical Shift left
01	AND
10	ADD



a) Design a one-bit ALU slice that performs these three operations. Use full adder, multiplexer, and basic logic gates as your building blocks. [4pts]



b) Connect four slices to get the required 4-bit ALU. [2pts]