1. What would happen if the CPU is servicing an interrupt while another I/O interrupt happens?

2. How does directed memory access (DMA) work? What benefit(s) does DMA bring compared to interrupt-driven I/O?
3. Describe the di↵erences between programmed I/O and memory-mapped I/O.

4. What is RTL:
5. Conditional Transfer between registers occurs only under a control condition Representation of a (conditional) transfer
    a. give an example

    b. Show Hardware implementation of a controlled transfer:

6. A bus system can be constructed with three-state buffer gates instead of multiplexers, explain ?
7. Which one of below instruction is read and which one is write from memory ?

    DR ← M[AR]
    M[AR] ← DR
8. microoperations :
    a. What are the main categories microoperations most often encountered in digital computers ?
    b. Give example for each operation ?
9. What is Random Access Memory (RAM) –
10. memory: can be characterized by 3 parameters, what are they ?
11. From what we learned in class, What can we do to To hide long memory access latency ?
12. What is Cache ?

13. What is
    a. Memory Hit:
    b. **Hit Rate:**
    c. **Hit Time:**
    d. Miss:
    e. **Miss Rate =**
    f. **Miss Penalty:**
14. A large enough miss penalty will cause a substantial decrease in CPU execute time, consider CPI = 1.0 when all memory accesses are hits. only data accesses are during loads and stores (50% of all instructions are loads or stores) miss penalty is 25 clock cycles, miss rate is 2% what is the impact on CPI?

15. To build a RAM IC from a RAM slice, we need