**ENCS2380 Computer Organization and Microprocessor**

**HW4**

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Q1:

It has arithmetic logic to do operations on data and registers to keep data in them

Q2:

It selects operations and instructions from main memory in a proper sequence and interprets them and does logic functions.

Q3:

The control unit provides it with signals.

Q4:

Clock frequency is the reciprocal of the clock cycle time but the clock cycle time is the duration the difference in time between two signals which synchronizes the circuits.

Q5:

Starting a program, providing the user interface (UI) and managing programs.

Q6:

A 64Kb.   
B 64Kb.   
C It uses the same address/data bus to access both the memory space and the I/O space. But there is an extra signal that tells whether the address/data is in the memory space or the I/O space.  
D The 8 bit IO bus allows 256 different addresses (2^8), so it will be a 256 addresses or 512 8-bit ports.

Q7:

Sequential accesses data in a linear sequence but the random access, the location can be selected randomly. However, the direct access has the data addressed based on physical location

Q8:

Faster access time, greater cost per bit; greater capacity, smaller cost per bit; greater capacity, slower access time.

Q9:

A CPU communication, control and timing, device communication, data buffering and error detection.

B All of them are slower. The I/O module interface employs Data Buffering to limit this speed mismatch.

Q10:

A

8 bits used to opcode, the remaining will be used to immediate operand, so it will be 2^24 which is equal to 16777216 Bytes.

B

The size of the data bus is the same which takes us to conclude that moving data between memory and CPU will be the same time

C

16

Q11:

A

The data is accepted by INPR if FGI =0, and if it is 1, the microprocessor will transfer the data, and the flag will become zero, when the data is getting ready to be transferred, the FGO flag is verified if the FGO is 1, the data is transferred to the OUTR, the FGI is 1 until the data is received.

B

The FGO keeps checking for the flags of FGI and FGO to see if the data is sent and received, IEN interrupt will be issued by teletype signal when the data is ready to get sent or received if the IEN interrupts are used

Q12:

Unfortunately, I can’t find any figure attached in the file.