Note: Exact copy will take zero for all. Use printed word doc or write a readable answers.

1. **Question 1:**
   a) Explain the difference between CMP and SUB instruction
   b) What is the last instruction in the procedure and what does it do?
   c) Select an instruction that adds BX to DX, and also adds the contents of the carry flag (C) to the result.
   d) If DL = 0F3H and BH = 72H , list the difference after BH is subtracted from DL and show the contents of the flag register bits
   e) List the five flag bits tested by the conditional jump instructions.
   f) Suppose that DS=1000H,BX=2000H, BP=1000H and DI=0100H. Determine the memory address accessed by each of the following instructions, assuming real mode operation:
      a) MOV AL,[BP+DI]
      b) MOV CX,[DI]
      c) MOV EDX,[BP]

   g) Suppose that DS=1200H,BX=0100H, SI=0250H and DI=0100H. Determine the address accessed by each of the following instructions, assuming real mode operation:
      a) MOV [100H],DL
      b) MOV [SI+100H],EAX
      c) MOV DL,[X+100H]

2. **Question 2:**

Develop a sequence of instructions that adds the 8-digit BCD number in AX and BX to the 8-digit BCD number in CX and DX. (AX and CX are the most significant registers. The result must be found in CX and DX after the addition.)

3. **Question 3:**

Develop a sequence of instructions that scans through a 300H-byte section of memory called LIST, located in the data segment, searching for a 66H.

4. **Question 4:**

Develop a sequence of instructions that searches through a block of 100H bytes of memory. This program must count all the unsigned numbers that are above 42H and all that are below 42H. Byte-sized data segment memory location UP must contain the count of numbers above 42H, and data segment location DOWN must contain the count of numbers below 42H.

5. **Question 5 - chapter 9**
   a) What happens when the HOLD input to the 8086/8088 is placed at its logic 1 level?
   b) Which bus connections on the 8088 microprocessor are typically demultiplexed?
   c) If the CLK input to the 8086/8088 is 4 MHz, how long is one bus cycle?
   d) How much time is allowed for memory access when the 8086/8088 is operated with a 5 MHz clock?
   e) What main function is provided by the 8288 bus controller when used with 8086/8088 maximum mode operation?

6. **Question 6:**
   a. List the number of data items stored in each of the following memory devices and the number of bits in each datum:
      a) 2K · 4
      b) 1K · l
      c) 4K · 8
      d) 16K · 1
      e) 64K · 4
   b. How many bytes of storage do the following EPROM memory devices contain?
      a) 2708
      b) 2716

c) 2732
d) 2764
e) 27512

7. **Question 7: A certain IBM 970 processor has a system clock frequency of 1.2 GHz. What is the clock period?**
8. **Question 8: Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.**
   a. What is the maximum directly addressable memory capacity (in bytes)?
   b. Discuss the impact on the system speed if the microprocessor bus has
      1. a 32-bit local address bus and a 16-bit local data bus, or
      2. a 16-bit local address bus and a 16-bit local data bus.
   c. How many bits are needed for the program counter and the instruction register?

9. **Question 9: Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:**
   INPR: Input Register, 8 bits
   OUTR: Output Register, 8 bits
   FGI: Input Flag, 1 bit
   FGO: Output Flag, 1 bit
   IEN: Interrupt Enable, 1 bit
   Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.
   a. Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.
   b. Describe how the function can be performed more efficiently by also employing IEN.

10. **Question 10: For a synchronous read operation (Figure 3.19), the memory module must place thedata on the bus sufficiently ahead of the falling edge of the Read signal to allow for signal settling. Assume a microprocessor bus is clocked at 10 MHz and that the Read signal begins to fall in the middle of the second half of T3.**
    a. Determine the length of the memory read instruction cycle.
    b. When, at the latest, should memory data be placed on the bus? Allow 20 ns for the settling of data lines.

11. **Question 11: The Intel 8088 microprocessor has a read bus timing similar to that of Figure 3.19, but requires four processor clock cycles. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle. Assume a processor clock rate of 8 MHz.**
    a. What is the maximum data transfer rate?
    b. Repeat but assume the need to insert one wait state per byte transferred.

12. **Question 12: Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.**

13. **Question 13: The microprocessor of Problem 3.14 initiates the fetch operand stage of the increment memory direct instruction at the same time that a keyboard actives an interrupt request line. After how long does the processor enter the interrupt processing cycle? Assume a bus clocking rate of 10 MHz.**