BIRZEIT UNIVERSITY

Electrical and Computer Engineering

ENCS2380 - Computer Organization and microprocessor

Fall 2021 - Midterm Exam

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Question	Max score	Score	ABET SO
1	15		
2	10		
3	10		
4	15		
Total	50		

Question #1 (15 Points): Choose the correct answer, and write the letter in the table below

1. The addressing mode in which the address of an instruction's operand is stored into a register

A. Register direct B. Register indirect C. Direct D. Indirect

2. The two's complement representation of **-15**:

A. 10001 B. 110001 C. 11110001 D. All of the above

3. The result of arithmetic right shift of 10100110 by 4 bits is:

A. 00000010 B. 000000100 C. 11111010 D. 001001101

4. One of the following affects the instruction count (IC) of the program

A. Compiler B. Instruction Format C. CPU clock rate D. CPI

5. There can be multiple computer organizations for the same computer architecture

A. True B. False

6. Which of the following is not a characteristic of a RISC architecture.

(A) Large instruction set (B) One instruction per cycle
(C) Simple addressing modes (D) Register-to-register operation

7. Assume that Memory[20] = 40
Memory [30] = 50
Memory [40] = 60
Memory [50] = 70

Which of the following instructions does not load 60 into the accumulator register

(A) Load immediate 60 (B) Load direct 30 (C) Load indirect 20 (D) both (A) & (C)

8. A Stack-organized computer uses instruction of

(A) Indirect addressing (B) Two-addressing

(C) Zero addressing (D) One addressing

9. What is the content of Stack Pointer (SP) register?

(A) Address of the current instruction (B) Address of the next instruction

(C) Address of the top element of the stack (D) Size of the stack

10. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

(A) Data transfer instructions. (B) Program control instructions.

(C) Input-output instructions. (D) Logical instructions

11. The basic principal of Von Neumann computer is storing program's code and data in two separated memories

(A) True (B) False

12. When calling subroutines, the return addresses are most appropriately stored in a stack memory

(A) True (B) False

13. The fetch-decode-execute cycle refers to the process (stages) by which data is read from the hard disk and stored in memory.

(A) True (B) False

14. Shift left the content of a register five bits is equivalent to divide it by 32.

(A) True (B) False

15. Interrupts can be generated in response to

(A) Detected program errors such as arithmetic overflow or division by zero

(B) Detected hardware faults (C) Input/output activities

(D) Internal timers (E) B, C, and D

(F) A, B, C, and D

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.

Answers of Question 1

Question #2 (10 Points):

Consider a processor to be developed having the following instruction formats as given below.

i. Register-Register instructions (R- type)

OpCode	Destination Reg.	Source Reg.1	Source Reg. 2 or Immediate No. (16 bits)
29 24	23 20	19 16	15 0

ii. Load-Store instructions (LS –type)

OpCode	Src/Dest Reg.	Memory Address
29 24	23 20	19 0

Determine the following parameters of the computer hardware to be designed.

1) **(3 points)** Maximum total number of instructions that can be implemented in this processor

The maximum number of instructions = maximum number of possible opcodes

Maximum number of possible opcodes = $2^{number\ of\ bits\ to\ represent\ opcode}$

$= 2^6 = 64$ instructions

2) **(3 points)** Maximum number of registers this processor can have.

The maximum number of registers = $2^{number\ of\ bits\ to\ represent\ register\ number}$

$= 2^4 = 16$ registers

3) **(4 points)** Assuming that a program can access data from any place in the main memory, determine the maximum size of the main Memory in Mbytes.

The maximum addressable memory size = $2^{number\ of\ bits}$ in the memory address

$= 2^{20} = 1$ MB

Question #3 (15 Points):

A memory, shown below, is used to store instructions and data for a basic machine with three 16-bit registers, namely, **R0, R1,** and **R2**. Moreover, this machine has **PC** and **IR** registers. Assume that the first instruction of a given program is stored at memory address location **100H**. All numbers are in Hexadecimal format.

Opcode (2bits)	Dest. Reg (2bits)	Memory Address (12bits)

Instruction format

2's complement Signed integers (16 bits)

Data format

Opcode 00 *is to load register Ri from the specified memory address*

Opcode 01 *is to store register Ri to the memory at the specified address*

Opcode 10 *is to add the content of register Ri to the content of the specified memory location and store the result in Ri*

Opcode 11 *is to subtract the memory content at the specified memory address from the content of register Ri and store the result in Ri*

Memory Address	100	101	102	103	104	105	106	107	108
Content	**1106**	**2107**	**9108**	**E108**	**5108**	**0001**	**0004**	**0005**	**0003**

	PC	**IR**	**R0**	**R1**	**R2**
Registers Initial Values	**100H**	**0000**	**0000**	**0000**	**0000**
After 1st instruction execution	**101H**	**1106**	**0000**	**0004**	**0000**
After 2nd instruction execution	**102H**	**2107**	**0000**	**0004**	**0005**
After 3rd instruction execution	**103H**	**9108**	**0000**	**0007**	**0005**
After 4th instruction execution	**104H**	**E108**	**0000**	**0007**	**0002**
After 5th instruction execution	**105H**	**5108**	**0000**	**0007**	**0002**

a) **(5 points)** Fill in the table above with the values for PC, IR, R0, R1 and R2 registers? Initial values mean the values of the registers prior to fetching the first instruction from memory.

b) **(2 points)** What is the range of the signed integer values that can be stored in this memory?

The data has 16-bit width

$-2^{n-1} \rightarrow 2^{n-1} - 1 \rightarrow -2^{15} \rightarrow 2^{15} - 1$

c) **(3 points)** write the machine code for the instruction **ADD R0, [105H].**

ADD has opcode of 10

R_0 is represented by 00

Thus, the machine code of is as follows:

$(1000\ 0001\ 0000\ 0101)_2$

$(8105)_{16}$

d) **(5 points)** Using the available above four instructions, write an assembly code to perform

Mem[105]=Mem[106]+Mem[107]

LOAD R_0, MEM [106] // load memory location 106 to register R_0

ADD R_0, MEM [107] // Add the content of memory location 107 to the //content of register R_0 and store the result in R_0

STORE R_0, MEM [105] // Store the content of R_0 to memory location 105

Question #4 (10 Points):

Use Booth's algorithm to perform **(8) x (-4)** using the minimum number of bits.

Minimum number of bits = 5

Assume 8 is the multiplier and (-4) is the multiplicand

Multiplier = 01000

Multiplicand = 2's complement of 4 = 11100

A	Q	Q0-1	M	Comments
00000	01000	0	11100	Shift
00000	00100	0		Shift
00000	00010	0		Shift
00000	00001	0		Subtract
00100	00001	0		Shift
00010	00000	1		Add
11110	00000	1		Shift
11111	00000	0		Final Answer