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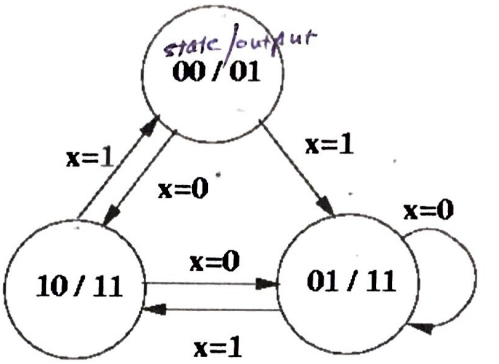
BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Electrical and Computer Engineering Department
ENCS533-Advanced Digital Design **Second Semester 2018/2019**

Final Exam **Duration: 120 minutes**
Instructor: Dr. Abdellatif S. Abu-Issa

Q1) (21 points)

a) For the following state diagram:



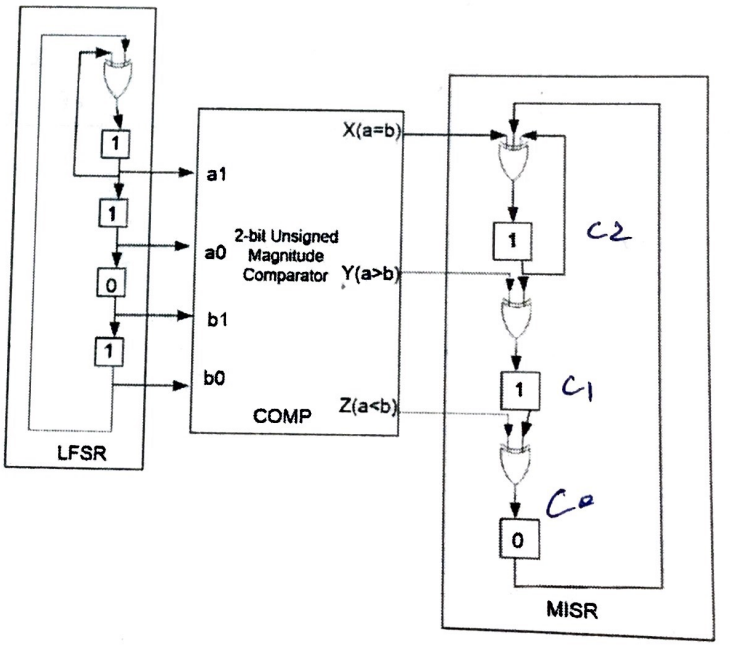
i) Is this Mealy or Moore Machine and Why? **[2 points]**
ii) Write a VHDL behavioural code to describe the circuit presented by the state diagram. **[12 points]**

b) Show the detailed diagram for the 4-bit LUT for F = A'B+C'D+AD'. **[7 points]**

Q2) (21 points)

The following figure shows a Built-In Self-Test Circuit for a 2-bit magnitude comparator. The test vectors are generated using a 4-bit LFSR and the results are analysed using a 3-bit MISR as shown in the figure.

a) Show the first 8 test vectors generated by the LFSR. The first vector of the LFSR is "1101", you should show the next 7 test vectors. **[6 points]**
b) What is the fault free signature of this system after we apply these test vectors? (Initial value of the MISR "110") **[9 points]**
c) Assume that the output Z(a<B) is Sa0. What is the signature after we apply the same test vectors generated by the LFSR? (Initial value of MISR is "110") **[6 points]**



Q3) (38 points)

a) Assign output values to the don't care states in the following flow table in such a way as to avoid transient output pulses. ***[4 points]***

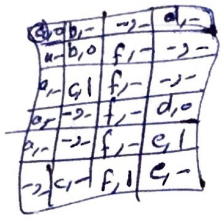
	00	01	11	10
a	(a),0	b, -	-, -	d, -
b	a, -	(b), 1	(b), 1	c, -
c	b, -	-, -	b, -	(c), 0
d	c, -	(d), 1	c, -	(d), 1

b) An asynchronous circuit with two inputs (x1 and x2) and one output (z). When both inputs are zeros (i.e. x1= x2 = 0) then z = 0, and when both inputs are ones (i.e. x1 = x2 = 1) then z = 1, otherwise the output will not change. Show the primitive follow table of this circuit. **[10 points]**

x_1x_2

	00	01	11	10
1	①/0	2/0	-/-	6/0
2	1/0	②/0	3/0	-/-
3	-/-	2/0	③/0	4/-
4	1/-	-/-	5/1	④/1
5	-/-	2/-	⑤/1	4/1
6	1/0	-/-	5/-	⑥/0

c) Given the following primitive flow table, draw the reduced flow table after reducing the number of states. **[12 points]**



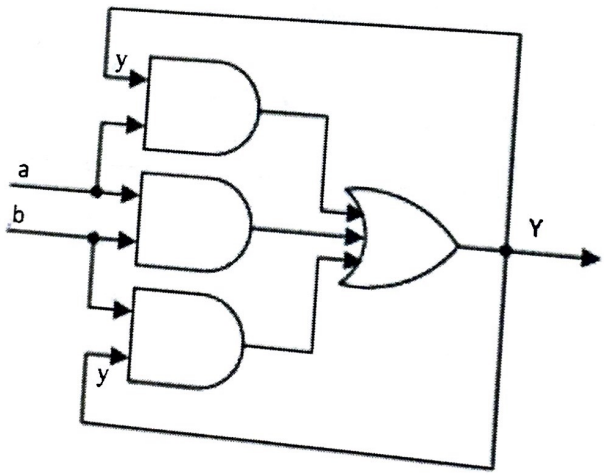
1, 2
1, 6
2, 3
4, 5

1,2	ⓐ/0	ⓐ/0	b/0	c/0
2,3	a/0	ⓑ/0	ⓑ/0	d/-
1,6	ⓒ/0	b/0	d/-	ⓒ/0
4,5	a/-	b/-	ⓓ/1	ⓓ/1

d) i) Show the transition table for the following circuit. **[3 points]**
ii) Implement the same circuit using SR-latch. Use NAND gates only in your design. **[9 points]**

$S = (a\,b)'$
$R = (a'\,b')'$

0	0	1	0
0	1	1	1



☺ Good Luck ☺