BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING
ELECTRICAL AND COMPUTER SYSTEMS ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN ENCS339

Midterm Exam — Second Semester 2004\2005

Time: 90 min.

Instructor: Abdellatif S. Abu-Issa

GIFT (6 points): Compare between ASICs, general-purpose computers, and FPGAs in the aspects of computation speed and flexibility. **Your answer should be in key points.**

1. **(a) (15 points):** A VHDL description is given below for a simple device that has 1 input **a** and 1 output **e.**

```
LIBRARY    ieee;
USE ieee.std_logic_1164.ALL;

ENTITY exam IS
      PORT
      (a: IN std_logic:='0';
      e: OUT std_logic);
END;

ARCHITECTURE question OF exam IS
SIGNAL b,c,d: std_logic:='0';
BEGIN

      --Statements to go here
END ARCHITECTURE ;
```

The input **a** is changed at some time from its initial value '0' to a new value '1'.
Three different versions of the body of the architecture which is labelled by (**-- Statements to go here**) are listed below, labelled (i) to (iii).
For each of the three versions explain what are the final values of signals b, c, d, and output e. **Justify your answer.**

(i)
```
PROCESS(a)
      BEGIN
      e<=c;
      c<=b;
      b<=a;
      d<=b;
END PROCESS;
```

(ii)
```
PROCESS(a,b)
      BEGIN
      e<=c;
      c<=b;
      b<=a;
      d<=b;
END PROCESS;
```

(iii)
```
PROCESS(a,b,c)
      BEGIN
      e<=c;
      c<=b;
      b<=a;
      d<=b;
END PROCESS;
```

(b) (20 points) The following figure shows a parallel input serial output communication device with an even parity. The behaviour of the device is as follows:

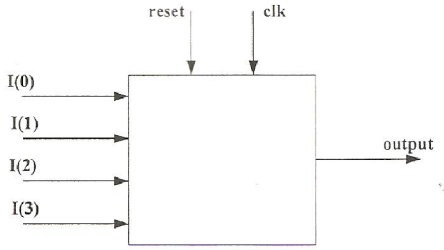
When reset = '1'

the output immediately becomes zero.

When reset ='0'

1) On the 1st rising clock edge, the value of I(0) appears in the output.
2) On the 2nd rising clock edge, the value of I(1) appears in the output.
3) On the 3ed rising clock edge, the value of I(2) appears in the output.
4) On the 4th rising clock edge, the value of I(3) appears in the output.
5) On the 5th rising clock edge, the value of the parity bit appears in the output.
6) The sequence then starts from step1.

Write a VHDL description for this device.

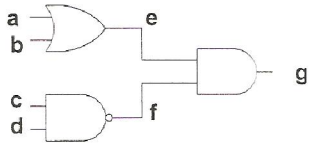


(c) (10 points): Our aim now is to make the communication device described in part (b) for n-bits instead of 4-bits. **Write a VHDL description for the n-bit device.**

(d)(10 points) Write a test bench for the device described in part (c) by instantiating the device for 6-bit input (i.e. n = 6).

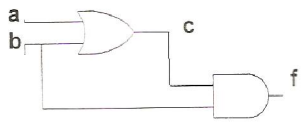
2.

a) **(25 points)** Use the following figure to answer the following questions

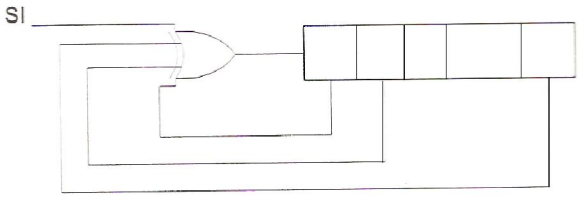


1. Use Boolean difference to find when the output g is sensitive to node a.
2. Use Boolean difference to find when the output g is sensitive to node c.
3. Find the test vectors for node a s-a-0 and s-a-1.
4. Find the test vectors for node b s-a-0 and s-a-1.
5. Find the test vectors for node c s-a-0 and s-a-1.
6. Find the test vectors for node d s-a-0 and s-a-1.
7. Find the test vectors for node e s-a-1.
8. Find the test vectors for node f s-a-1.
9. Find one test vector that can test node g for s-a-1.

b) (10 points): Use the D-algorithm sensitive path method to find test vectors for c s-a-0 and s-a-1 in the figure below.



c) (15 points): The signature analyser shown below is initialised to the all-zero state, and then is fed with the data stream 110110111 to the SI input (LSB comes first)



1. What is the fault free signature?
2. Show that if the fifth bit is in error, then the signature will be different from the fault free case.

GOOD LUCK