‘Advance Digital ‘

‘Home work 1 ‘

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```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY mux4_1 IS
        PORT(
        d : IN std_logic_vector(3 DOWNTO 0);
        s : IN std_logic_vector(1 DOWNTO 0);
        y : OUT std_logic

        );
END;

ARCHITECTURE mux41 OF mux4_1 IS
BEGIN

        y <= d(0) WHEN s = "00"
        ELSE d(1) WHEN s = "01"
        ELSE d(2) WHEN s = "10"
        ELSE d(3) WHEN s = "11"          ;

END ;
```

```
-- ************************************************************
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY mux2_1 IS
        PORT(
        d : IN std_logic_vector(1 DOWNTO 0);
        s : IN std_logic;
        y : OUT std_logic

        );
END;

ARCHITECTURE mux21 OF mux2_1 IS
BEGIN

        y <= d(0) WHEN s = '0'
        ELSE d(1) WHEN s = '1';

END ;

-- ********************************
 LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY mux8_1 IS
        PORT(
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        d : IN std_logic_vector(7 DOWNTO 0);
        s : IN std_logic_vector(2 DOWNTO 0);
        y : OUT std_logic

        );

END;


ARCHITECTURE mux81 OF mux8_1 IS
SIGNAL n:std_logic_vector(1 DOWNTO 0);
BEGIN

        g1: ENTITY work.mux4_1(mux41)
                PORT MAP (d(3 DOWNTO 0) , s(1 DOWNTO 0),n(0)) ;


        g2: ENTITY work.mux4_1(mux41)
                PORT MAP (d(7 DOWNTO 4) , s(1 DOWNTO 0),n(1)) ;

        g3:     ENTITY work.mux2_1(mux21)
                PORT MAP (n(1 DOWNTO 0),s(2),y) ;


END ;
```

```
-- ************************************************
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY test IS
END ;

ARCHITECTURE testmux OF test IS
SIGNAL d:std_logic_vector(7 DOWNTO 0) ;
SIGNAL s:std_logic_vector(2 DOWNTO 0) ;
SIGNAL y:std_logic ;
BEGIN

        g1:ENTITY work.mux8_1(mux81)
                PORT MAP(d,s,y);



                d <= x"82";

                s <= "000",
                "001" AFTER 10 ns ,
                "010" AFTER 20 ns ,
                "011" AFTER 30 ns ,
                "100" AFTER 40 ns ,
                "101" AFTER 50 ns ,
                "110" AFTER 60 ns ,
                "111" AFTER 70 ns ;

END;
```

Sample of simulation :