BIRZEIT UNIVERSITY

ENCS533 - Advanced Digital Design

Homework# 1

★ ★

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Section 2

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Code:

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY MUX21 IS
    PORT( a:IN STD_logic_vector(1 DOWNTO 0);
          s:IN STD_LOgic;
          w:OUT STd_logic
    );
END MUX21;

ARCHITECTURE MUX21 OF MUX21 IS
BEGIN
w <= a(0) WHEN s='0'
ELSE a(1) WHEN s='1';
END MUX21;
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY MUX41 IS
    PORT( c:IN std_logic_vector (3 DOWNTO 0);
          s:IN std_logic_vector (1 DOWNTO 0);
          z: OUT std_logic
          );
END MUX41;

ARCHITECTURE MUX41 OF MUX41 IS
BEGIN
z <= (NOT s(1) AND NOT s(0) AND c(0))
  OR (NOT s(1) AND     s(0) AND c(1))
  OR (     s(1) AND NOT s(0) AND c(2))
  OR (     s(1) AND     s(1) AND c(3));
END MUX41;
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY MUX81 IS
    PORT( d:IN std_logic_vector (7 DOWNTO 0);
    s:IN std_logic_vector (2 DOWNTO 0);
    y:OUT std_logic
    );
END MUX81 ;

ARCHITECTURE MUX81 OF MUX81 IS
SIGNAL result: std_logic_vector(1 DOWNTO 0);
BEGIN
    M1:ENTITY work.MUX41(MUX41) PORT MAP ( d(3 DOWNTO 0), s(1 DOWNTO 0),result(0)) ;
    M2:ENTITY work.MUX41(MUX41) PORT MAP ( d(7 DOWNTO 4), s(1 DOWNTO 0),result(1));
    M3:ENTITY work.MUX21(MUX21) PORT MAP (result(1 DOWNTO 0),s(2),y);
END MUX81;
```

```
54  LIBRARY IEEE;
55  USE IEEE.STD_LOGIC_1164.ALL;
56  ENTITY mytestbench IS
57  END mytestbench ;
58
59  ARCHITECTURE test OF mytestbench IS
60  SIGNAL mux_inputs: std_logic_vector (7 DOWNTO 0);
61  SIGNAL mux_Selctors: std_logic_vector (2 DOWNTO 0);
62  SIGNAL mux_out: std_logic;
63
64  BEGIN
65      M1: ENTITY work.MUX81(MUX81) PORT MAP (d=>mux_inputs, s=>mux_Selctors, y=>mux_out);
66          mux_inputs <="10101011";
67          mux_Selctors <= "111",
68          "110" AFTER 30 ns,
69          "101" AFTER 60 ns,
70          "010" AFTER 90 ns;
71  END;
```

Simulation: