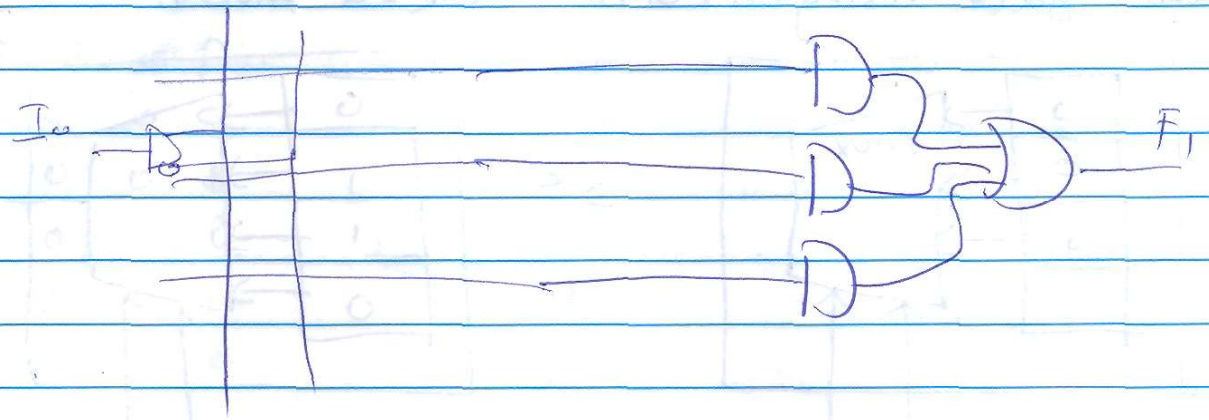
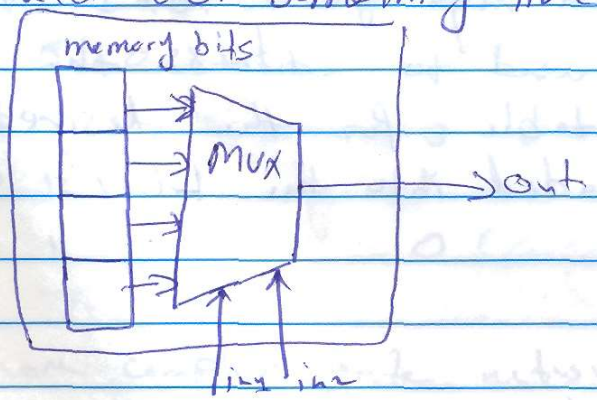
(3) PAL : (Programmable Array Logic)



(*) FPGAs (Field Programmable Gate Array)

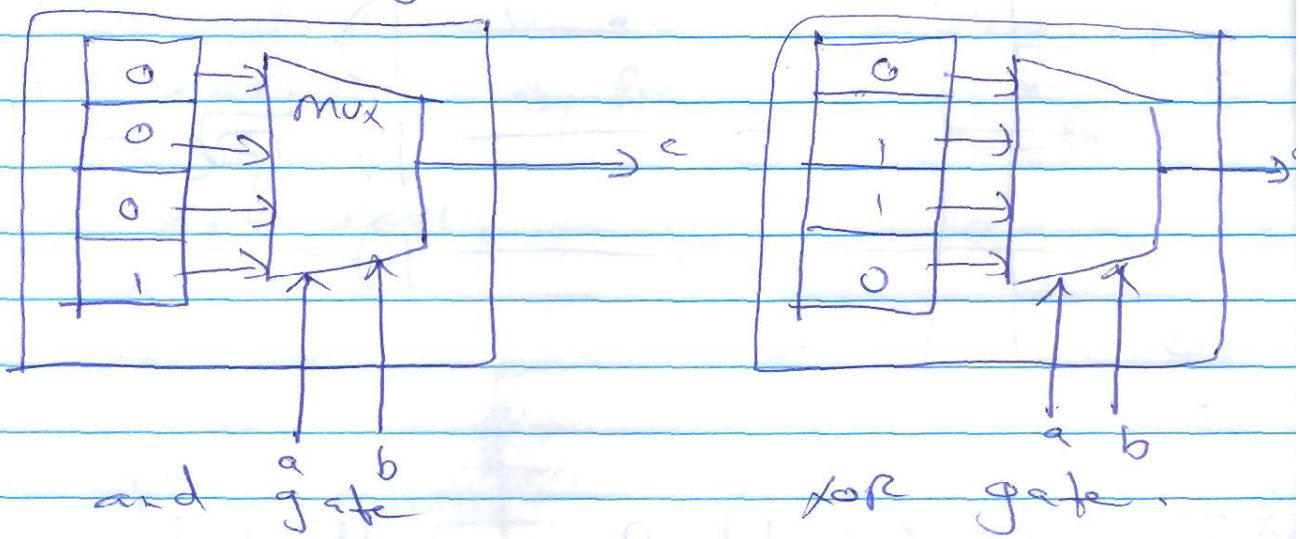
- FPGAs is usually based on a look-up table (LUT) approach.

For example a two input programmable logic gate would look something like this



In this example, the look up table (LUT) is a series of four memory bits. The two inputs (In1 & In2) select one of the memory bits to be fed to the output.

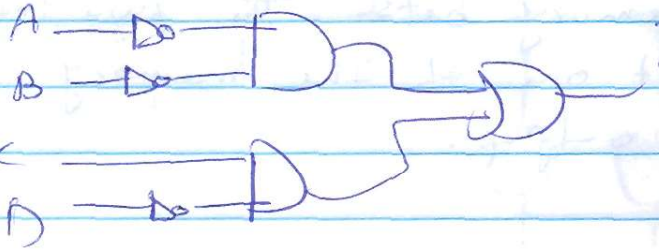
For example if we want to implement an and gate using FPGA c <= a AND b.



⊛ For example in ALTERA FLEX 10K, the gate ~~level~~ logic is implemented using a (LUT). The LUT is a high speed 16 x 1 SRAM.
⇒ Four inputs are used to address the LUT memory. The truth table for the desired gate network is loaded into the LUT's SRA during programming.

Ex:

$$F = A'B' + CD'$$



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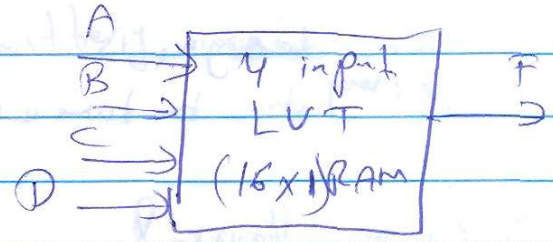
∴ RAM Contents

Address				Data
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



⊛ more complex gate networks can be fed to a D flip-flop and then to interconnection network