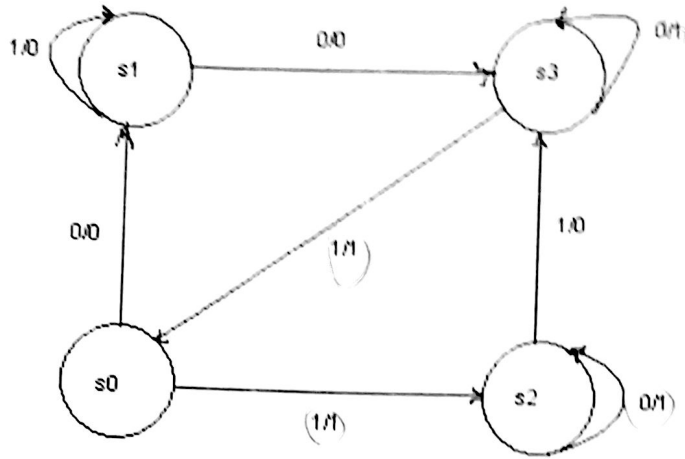


Q1) 20 points (14 + 6)

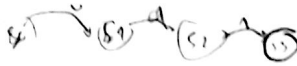
a) Figure 1 shows a Mealy FSM. At any time the reset input is pressed (reset = '1') then the machine will go to S0 and the output is 0. Otherwise, the machine will work as specified in the state diagram in Figure 1. Write a behavioural VHDL description for this Mealy FSM



$x \oplus xy + x'y +$
 $x'(y+1)$
 $0 + xy + x'y + 0$

Figure 1: Question1 Mealy FSM

b) Show the Moore state diagram for a sequence detector circuit that has one input x and output z. The output z is 1 when the sequence "001" is detected in the input x in 3 consecutive clock cycles. Otherwise the output is 0.



Q2) 26 points (12 + 12 + 2)

For the circuits shown in Figure 2

- a) Use D-algorithm to find all test vectors for b s-a-0 and b s-a-1
- b) Use Boolean difference to find all test vectors for Y s-a-0 and Y s-a-1
- c) Is the test vector XYZ = "101" can detect the fault F s-a-1

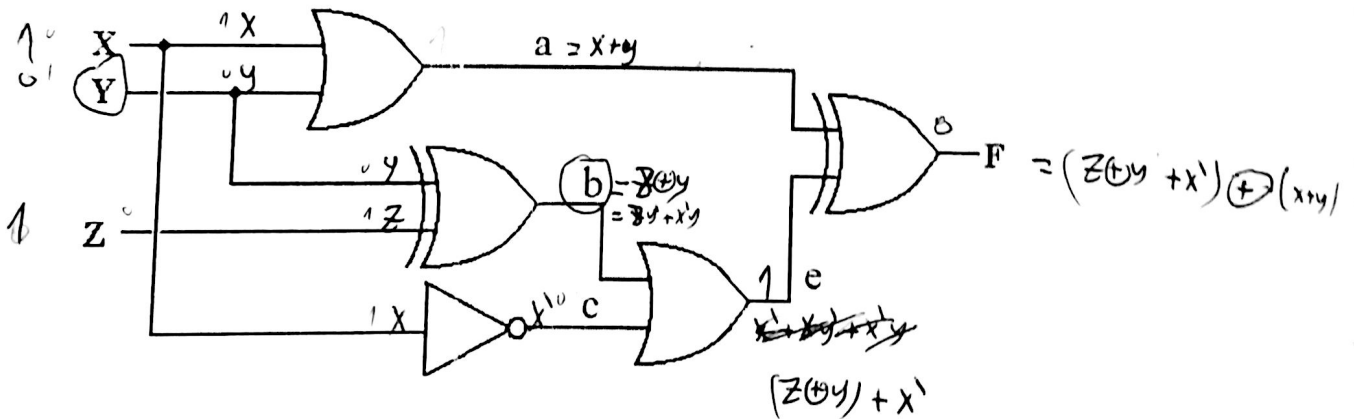


Figure 2: Question 2 Circuit

$c = \overline{x}$

000

3) 54 points (6 + 8 + 40)

a) Assign output values to the don't care states in the flow table shown in Figure 3 in such a way as to avoid transient output pulses and keeping the design minimized.

	00	01	11	10
a	(a), 0	b, -	-, -	d, -
b	a, -	(b), 1	(b), 1	c, -
c	b, -	-, -	b, -	(c), 0
d	c, -	(d), 1	c, -	(d), 1

Figure 3: Flow Table for Q3 part a

b) For the circuit shown in Figure 4

- i) Determine the values of inputs at which hazard may occur.
- ii) Draw the hazard-free circuit (OR-AND Implementation).

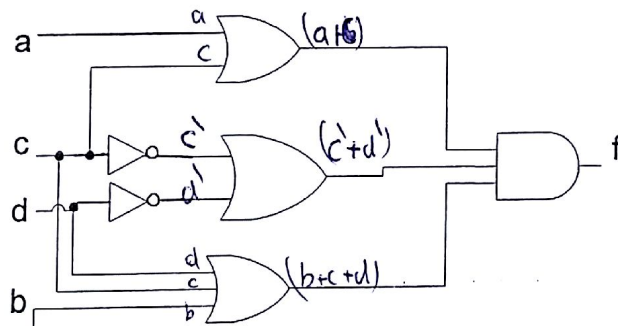


Figure 4: Question 3 part b

c) Use the asynchronous design procedure to design a **JK Latch**. The JK latch has 2 inputs (JK) and one output Q. It simply works as follows: If JK=00 the $Q^+ = Q$, if JK = 01 then $Q^+ = 0$, if JK=10 the $Q^+ = 1$ and finally if JK = 11 then $Q^+ = \text{not } Q$. Go through the steps of asynchronous design to

- 1) Get the primitive flow table. (12)
- 2) Get the reduced flow table. (12)
- 3) Get the race-free transition table. (2)
- 4) Get the glitch free output equation. (2)
- 5) Implement the circuit using SR latches (It is only allowed to use NAND gates in your implementation). (12)

00
10 4

☺ Good Luck ☺

J k
0 0
c 1
1 0
s=0
->4-10